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Design of Enhancement Mode Single-gate and Double-gate Multi-channel GaN HEMT with Vertical Polarity Inversion Heterostructure

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***Abstract*—We propose the design and simulation study of novel gallium nitride (GaN) devices, consisting of nitride stacks with different polarity, to provide multiple channels by flexible gate(s) control. Calibrated TCAD device simulations visualize device characteristics of 0.62-µm-gate-length multi-channel transistors. E-mode operations demonstrate a positive small threshold voltage V_{th} below 2 V at V_{ds} = 0.1 V for all multi-channel devices, and a high on-state current I_{on} (V_{gs} = V_{ds} = 4 V) up to 4 A/mm achieved by 4 channels induced within the device.**

I. INTRODUCTION

GaN HEMTs, a promising candidate of power electronic devices, have demonstrated higher power density and efficiency than conventional silicon and gallium arsenide based solutions [1]. In the past, the research efforts in GaN semiconductor device had mainly focused on Ga-polar GaN HEMTs. Recently, N-polar GaN, which has a reverse polarization field, shows the advantage over Ga-polar material in making enhancement mode (E-mode) device with low access resistance [2].

To further improve device power capabilities of GaN HEMTs, the development of double channels in GaN devices has been explored. The Ga-polar and lately the N-polar double-channel GaN HEMTs have been demonstrated by HKUST [3] and MERL [4], respectively. However, the former requires strong gate control for the lower channel and it is not capable of E-mode operation; the latter, addressing the issues of Ga-polar counterpart, but may suffer from mobility degradation due to possible channels overlap within one GaN layer [5].

To achieve E-mode GaN transistors with both higher current-carrying capacity and enhanced gate control, in this paper, we propose the design and study of multiple-channel GaN devices through integration of Vertical Polarity Inversion Heterostructures (VPIH), deliberate GaN stack layering and possible double-gate structure. In this work, the adopted VPIH structures, demonstrated by Mishra's group, realize polarity inversion through AlOx interlayer [6] or Mg+N treatment [7].

II. DEVICE STRUCTURE AND DESIGN

A. Double-gate Multiple-channel GaN HEMT with VPIH

Aiming at the equal gate control of the channel, a double-gate structure is utilized to ensure the gate controllability for device operation. To minimize the gate interference, VPIH structure with insulator interlayer is employed [6]. The nitride stacks are separated by the 30-nm-thick AlOx layer and thereby two quasi-independent systems are available for band engineering of each GaN stacks.

As shown in Fig. 1(a), by design of a Ga-polar AlN/GaN/AlN (3/20/3 nm) sandwich in the top stack, a corresponding vertical flip for the lower part with the same dimension, and a double-gate structure, two 2DEG channels can be developed in different polarity GaN layers under E-mode operation.

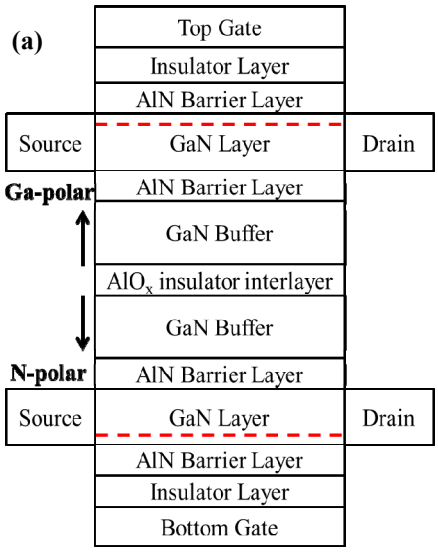

Fig. 1(a): Cross-sectional schematic of double-gate double-channel GaN HEMT-type device, which integrates upper Ga-polar and lower N-polar stacks through AlOx interlayer.

The channel generation is illustrated through simulated band diagrams as shown in Fig. 1(b). As V_{gs} increases, the 2DEG quantum wells approach and dip into the corresponding electron quasi-Fermi levels. Also as demonstrated in the device input characteristics (see Fig. 1(c)), two peaks of transconductance, indicates the development of two channels. It should be noted that the voltage difference between two peaks is less than 1 V.

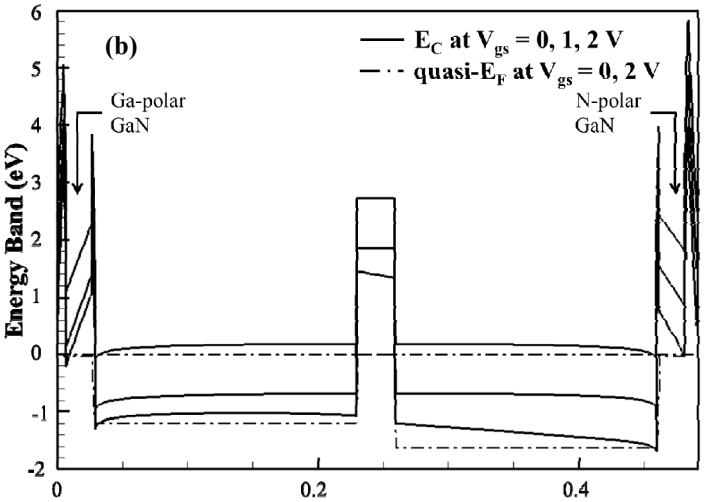

Fig. 1(b): The double-gate double-channel GaN HEMT-type device is capable of E-mode operation as observed in band diagrams; the gate workfunction is 4.4 eV.

Fig. 1(c) and Fig. 1(d) show the device input and output characteristics under the symmetrical gate control. V_{th} and g_{max} are obtained respectively as 1.67 V and 190 mS/mm under the drain bias of 0.1 V. The drive current I_{on} (V_{gs} = V_{ds} = 4 V) is boosted to 2.96 A/mm.

B. Double-gate Quadraple-Channel GaN HEMT with VPIH

Suggested by MERL's single-gate dual-channel GaN MIS-HEMT [4], by optimizing the gate dielectric layer and the sandwich stack, additional inversion carrier channels can be induced with good channel confinement towards quadruple conduction paths development in our double-gate HEMT with VPIH. In the TCAD simulation, we set both the Ga-polar and N-polar AlN/GaN/AlN stacks to be 2/20/2 nm, and the gate dielectric to be 1 nm. Assuming no gate leakage, as indicated by the surface conduction band bending in simulated band diagrams (see Fig. 2(b)), four quantum wells can be formed as applied gate voltage increases, two of which are inversion layers (blue dotted lines). Fig. 2(c) and Fig. 2(d) show device input and output device characteristics under the symmetrical gate control. The gate workfunction is tuned to suppress kink effects, and therefore V_{th} and g_{max} are obtained respectively as 0.9 V and 190 mS/mm, under the drain bias of 0.1 V. It is noted that obtained I_{on} is enhanced to 4.0 A/mm, but not twice of the double-channel device. This is due to the mobility degradation caused by channel overlap within GaN layers.

It should be noted that these double-gate devices are also capable of depletion mode (D-mode) operation through manipulating the layering of GaN stacks, combined D- and E-mode operation, and multiple channel development with flexible gate control (will be discussed in another paper).

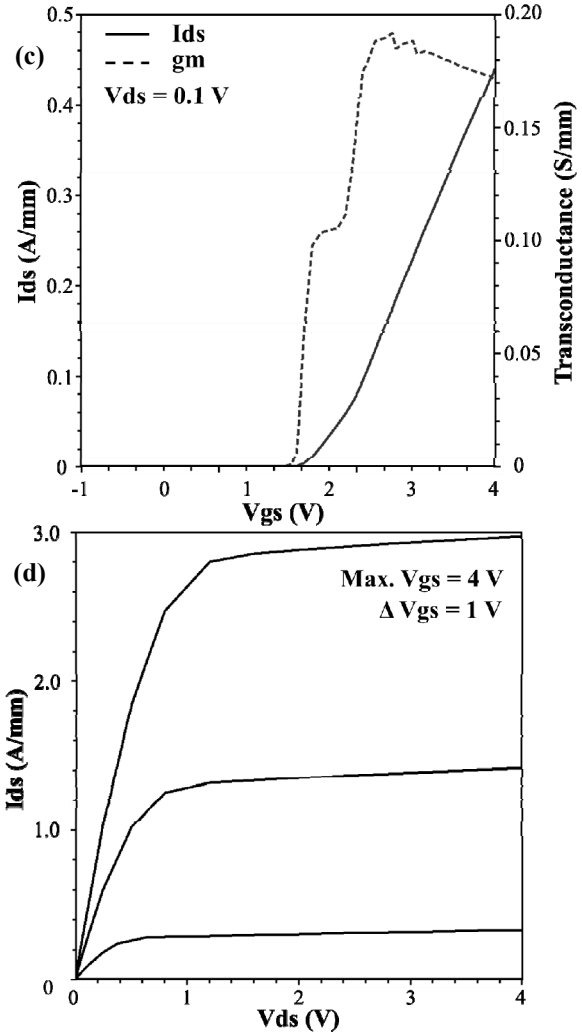

Fig. 1(c)(d): Input (c) and output (d) characteristics of the double-channel device. Max. g_m of 190 mS/mm and V_{th} of 1.6 V are obtained at V_{ds} = 0.1 V. Max. I_{on} is up to 3 A/mm.

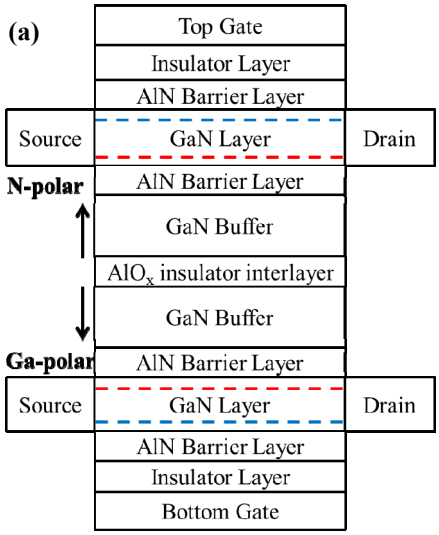

Fig. 2(a): Cross-sectional schematic of double-gate quadruple-channel GaN HEMT-type device with upper N-polar and lower Ga-polar stacks.

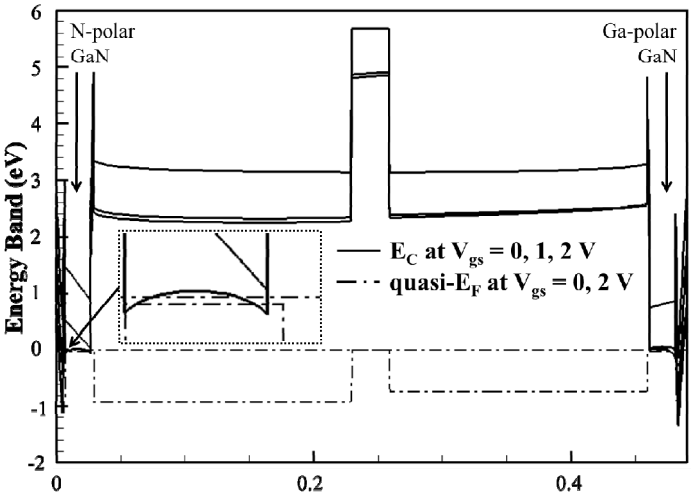

Fig. 2(b): The double-gate quadruple-channel GaN HEMT-type device can develop two quantum wells due to surface conduction band bending and another two due to heterojunction.

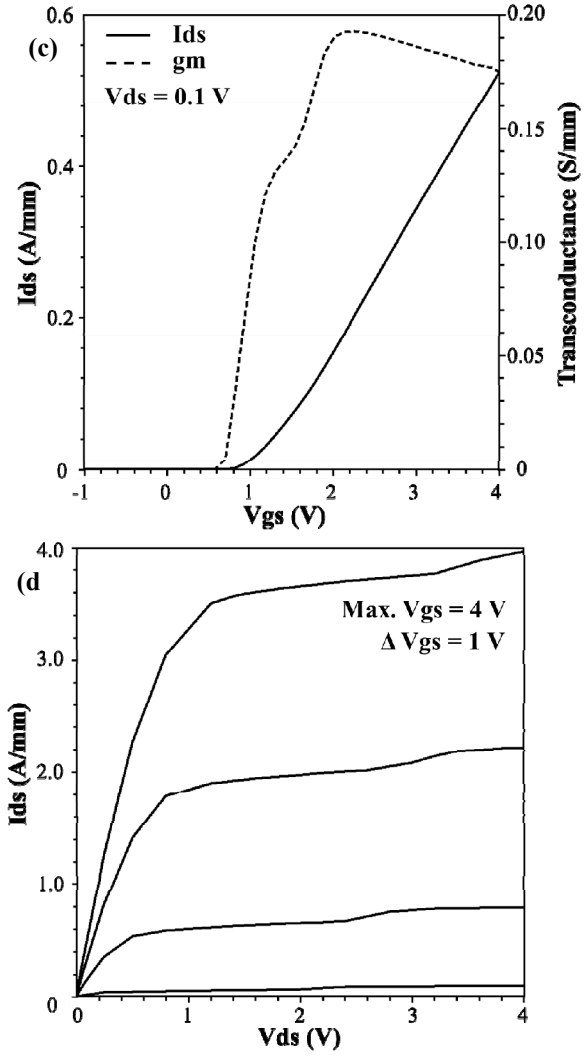

Fig. 2(c)(d): Input (c) and output (d) characteristics of the quadruple-channel device. Max. g_m of 190 mS/mm and V_{th} of 0.9 V are obtained at V_{ds} = 0.1 V. Max. I_{on} is up to 4 A/mm.

C. Single-gate Triple-Channel GaN HEMT with VPIH

In addition to double-gate structure, we propose a single-gate multiple-channel GaN HEMT (Fig. 3(a)) to reduce complexity in device fabrication. For this VPIH, N-polar stack is grown on Ga-polar stack by careful Mg+N treatment [7].

In TCAD simulation, we insert tuned p-type fixed charge at the polarity inversion interface to take into account of this physical effect. AlN layers in the N-polar sandwich are made thin for enhanced gate control of lower channels. The dimensions are 2/20/2 nm for N-polar and 3/30/3 nm for Ga-polar stacks. Meanwhile, an additional inversion channel (blue dotted line) can be introduced into the N-polar GaN layer to constitute triple conduction paths as indicated in Fig. 3(b) band diagrams, where the heterojunction 2DEG and the inversion carrier quantum wells approach quasi-Fermi level in sequence. Device input and output characteristics shown in Fig. 3(c)(d) indicate g_{max} of 110 mS/mm and V_{th} of 0.23 V at V_{ds} = 0.1 V. The on-state current I_{on} reaches is 1.18 A/mm. This low drive current may be due to the p-type dopants at the polarity inversion interface offsetting the polarization charges and thereby reduced 2DEG density.

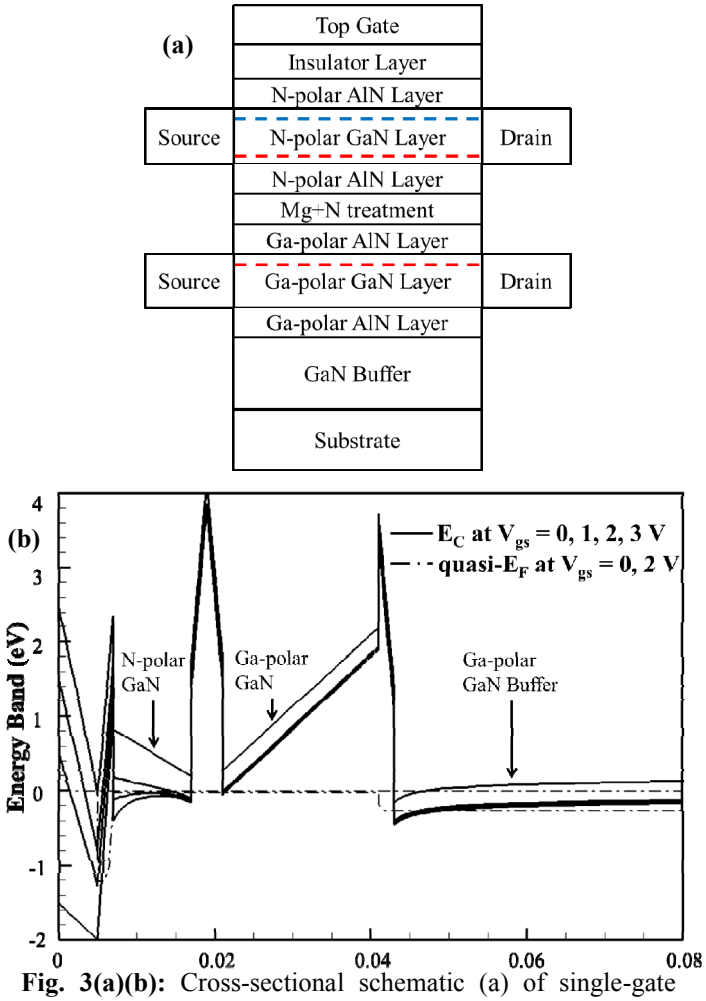

Fig. 3(a)(b): Cross-sectional schematic (a) of single-gate triple-channel GaN HEMT-type device integrating upper N-polar and lower Ga-polar stacks through Mg+N treatment. It is capable of E-mode operation and hybrid channels development as shown in (b) band diagrams under the gate.

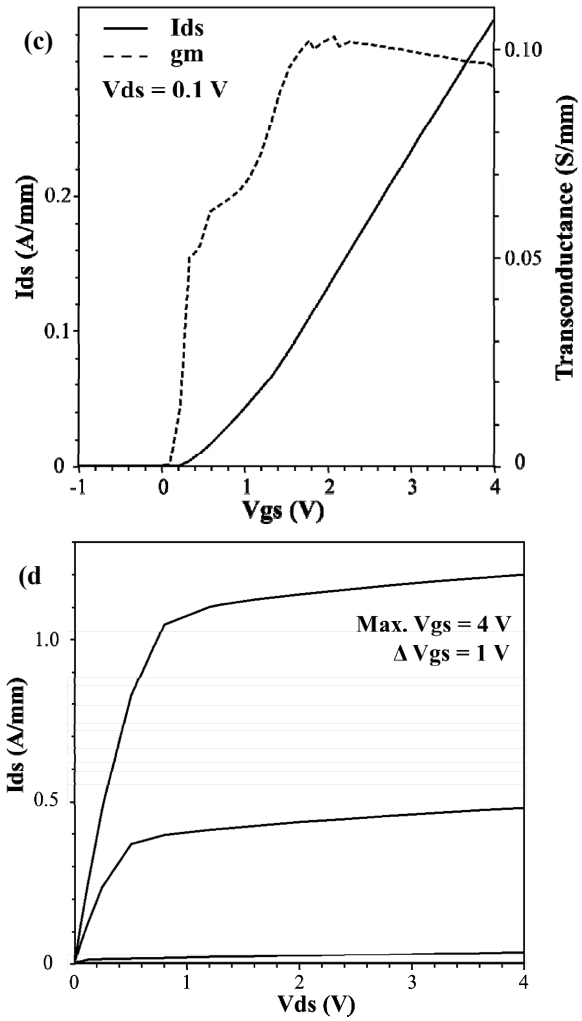

Fig. 3(c)(d): Input (c) and output (d) characteristics of the tripe-channel device. Max. g_m of 110 mS/mm and V_{th} of 0.23 V are obtained at V_{ds} = 0.1 V. Max. I_{on} is up to 1.2 A/mm.

III. CONCLUSION

We have demonstrated design methods of E-mode multiple-gate multiple-channel GaN HEMTs with VPIH structure. The mechanism for the creation of the multiple carrier channels has been identified. TCAD simulation results show that the drive current can reach 4A/mm. Also, the gate control of lower channels is strengthened in all three different device structures, where the voltage difference of g_m peak is less than 1 V. In addition, the double-gate devices are capable of combined E- and D-mode operation with flexible channel controls. All these positive features and significant performance improvement suggest that our novel GaN HEMT with VPIH structure can be a promising device structure for RF/power technologies application.

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