MITSUBISHI ELECTRIC RESEARCH LABORATORIES
http://www.merl.com

A Fast and Generalized Space Vector PWM Scheme and Its Application in Optimal Performance Investigation for Multilevel Inverters

Deng, Y.; Teo, K.-H.; Harley, R.G.

TR2013-084 September 2013

Abstract

This paper introduces and develops a fast and generalized space vector pulse width modulation (SVPWM) scheme and applies the SVPWM scheme to investigate the optimal performance of multilevel inverters. Due to the development in this paper, the introduced SVPWM scheme is more efficient when the commanded reference vector is in low modulation regions. The SVPWM scheme generates all the available switching states and switching sequences based on two simple and general mappings, and calculates the duty cycles simply as for two-level SVPWM, thus independent of the level number of the inverter and providing significant flexibility for analyzing and designing multilevel inverters. Because the switching states, duty cycles, and switching sequences are all obtained by simple calculation in the SVPWM scheme, no lookup table is needed and the scheme is computationally fast. In this paper, the performance of multilevel inverters is quantitatively analyzed according to different influencing factors, such as switching frequency, level number of the inverter, modulation index, and switching pattern. Simulation results and general conclusions are given.

IEEE Energy Conversion Congress & Expo (ECCE)

A Fast and Generalized Space Vector PWM Scheme and Its Application in Optimal Performance Investigation for Multilevel Inverters

Yi Deng[1, 2], Koon Hoo Teo[1], Ronald G. Harley[2]

[1]Mitsubishi Electric Research Laboratories, Inc.
201 Broadway, 8th Floor
Cambridge, MA 02139, USA
teo@merl.com

[2]School of Electrical and Computer Engineering
Georgia Institute of Technology
Atlanta, GA 30332, USA
{ydeng35, rharley}@gatech.edu

***Abstract*— This paper introduces and develops a fast and generalized space vector pulse width modulation (SVPWM) scheme and applies the SVPWM scheme to investigate the optimal performance of multilevel inverters. Due to the development in this paper, the introduced SVPWM scheme is more efficient when the commanded reference vector is in low-modulation regions. The SVPWM scheme generates all the available switching states and switching sequences based on two simple and general mappings, and calculates the duty cycles simply as for two-level SVPWM, thus independent of the level number of the inverter and providing significant flexibility for analyzing and designing multilevel inverters. Because the switching states, duty cycles, and switching sequences are all obtained by simple calculation in the SVPWM scheme, no lookup table is needed and the scheme is computationally fast. In this paper, the performance of multilevel inverters is quantitatively analyzed according to different influencing factors, such as switching frequency, level number of the inverter, modulation index, and switching pattern. Simulation results and general conclusions are given.**

***Keywords*— Space vector modulation; SVPWM; multilevel inverter**

I. INTRODUCTION

Multilevel inverters are widely used in high-power high-voltage applications due to their advantageous performance compared to two-level inverters. Several designable factors, such as switching frequency, level number of the inverter, modulation index, and switching pattern, can influence the performance of multilevel inverters. In order to achieve the optimal design of a multilevel inverter, quantitative analysis of its performance is necessary.

Space vector pulse width modulation (SVPWM), also called space vector modulation (SVM), is one of the most attractive modulation strategies for multilevel inverters [1]-[5]. However, in spite of its significant advantages, SVPWM for more than three-level inverters is still hardly explored, due to the largely increased number of switching states and switching sequences that accompany the higher number of levels.

Several SVPWM schemes [1]-[5] are known for three-level inverters. However, those schemes are not readily extended to four or higher level. One method partitions the three-level space vector diagram into six two-level space vector diagrams [1]. However, the axes of the *d-q* plane need to be rotated by a certain angle in each calculation of the reference vector location and thus the method is not easily applied to higher level inverters; and no general method for switching sequence selection or application for four or higher level inverter is introduced. A similar method for three-level inverters is described in [2], in which a two-phase to three-phase conversion is needed to calculate the shift of origin of a virtual two-level inverter. Since the two-phase to three-phase conversion is needed for each division of the space vector diagram, both the complexity and computation of this scheme will increase when applied to a four or higher level inverter. Moreover, no general switching sequence selection method is introduced either. A Euclidean vector system based SVPWM algorithm is presented in [3]. However, several matrix transformations are needed, and no systematic approach for determining the switching states or real-time implementation is provided. A coordinate transformation and switching sequence mapping based SVPWM scheme is proposed in [4], in which a coordinate transformation is needed to determine the location of the reference vector and to calculate the duty cycles, and a pre-stored switching sequence mapping table is needed to determine the switching sequence. Since the number of possible switching sequences increases sensitively with the increasing level of the inverter, more memory will be needed and slower mapping speed will be achieved when the method in [4] is applied to higher level inverters. In [5], the equivalent two-level sub-hexagon is detected, which contains the tip of the reference vector in the space vector

diagram of the multilevel inverter, and then the origin of the reference vector is relocated to the center of the two-level sub-hexagon. However, some switching states and switching sequences that are actually suitable for the reference vector are ignored in this method, which causes the method to not provide optimal switching waveforms for every operation condition.

This paper in Section II introduces and develops a fast and generalized SVPWM scheme for multilevel inverters, which can generate all the available switching states and switching sequences and calculates the duty cycles simply as for two-level SVPWM, thus providing significant flexibility for exploring the optimal performance of multilevel inverters. Based on this SVPWM scheme, Section III evaluates the performance of multilevel inverters according to different influencing factors, such as switching frequency, level number of the inverter, modulation index, and switching pattern. Finally, Section IV concludes the paper.

II. SVPWM SCHEME

The principle of the SVPWM scheme is illustrated in Fig. 1 based on the space vector diagram H_0 of a five-level inverter. Fig. 1(a) shows how to locate the reference vector $\boldsymbol{V}_{ref}$, i.e., to detect the modulation triangle $\Delta P_1P_2P_3$; Fig. 1(b)-(c) show how to calculate the duty cycles and to generate the switching sequences in two modes, i.e., counterclockwise (*mode*=1) and clockwise (*mode*=2), as if it were an equivalent two-level SVPWM. More details of this SVPWM scheme can be found in [6].

In order to synthesize or equate the reference vector, it is the task of the SVPWM scheme to detect the nearest three vectors $\boldsymbol{V}_{n1}$, $\boldsymbol{V}_{n2}$, and $\boldsymbol{V}_{n3}$ (i.e., the vectors from the center of H_0 to vertices P_1, P_2 and P_3), to determine the sequence of the nearest three vectors during a switching cycle (i.e., the switching sequence), and to calculate the needed on-time (i.e., duty cycle) of each nearest vector based on the following equation [3]

$$\boldsymbol{V}_{ref} = (n-1)\left(V_a^* + V_b^* \cdot e^{j\frac{2}{3}\pi} + V_c^* \cdot e^{j\frac{4}{3}\pi}\right) \quad (1a)$$

$$T_s \cdot \boldsymbol{V}_{ref} = d_1 \cdot \boldsymbol{V}_{n1} + d_2 \cdot \boldsymbol{V}_{n2} + d_3 \cdot \boldsymbol{V}_{n3} \quad (1b)$$

where V_a^*, V_b^*, and V_c^* are the command reference voltage of phase A, B, and C; T_s is the commanded switching cycle; and d_1, d_2, and d_3 are the duty cycles of $\boldsymbol{V}_{n1}$, $\boldsymbol{V}_{n2}$, and $\boldsymbol{V}_{n3}$, respectively.

The detailed method of generating the switching sequences and calculating the corresponding duty cycles, and the development of the SVPWM scheme when the reference vector locates in low-modulation regions, are introduced as follows.

A. Switching Sequences

First, the reference vector $\boldsymbol{V}_{ref}$ is represented as the sum of a set of "vertex vectors" (shown as blue solid arrows) and a "remainder vector" $\boldsymbol{V}_{ref}'$, as shown in Fig. 1(a). A vertex vector is a vector connecting two adjacent vertices. The remainder vector is the vector enclosed by the modulation triangle $\Delta P_1P_2P_3$ and connecting a first vertex (i.e., P_2 in Fig. 1(a)) of the modulation triangle with the reference vector.

One way to determine the set of vertex vectors is based on determining a set of nested hexagons H_1, H_2, and H_3 enclosing the reference vector, as shown in Fig. 1(a). Each nested hexagon corresponds to a specific level ranging from (n-1) to a second level, and centers at the vertex of a vertex vector. For instance, the method of selecting the nested (n-1)-level hexagon H_1 is shown in Fig. 2.

There are six vertex vectors available for the nested (n-1)-level hexagon H_1, i.e., the one blue solid arrow and five blue dashed arrows as shown in Fig. 2. The actual vertex vector, among the six available vertex vectors, for the nested (n-1)-level hexagon H_1, is the one for which the angle between this vertex vector and the reference vector is the smallest. In this way, the first vertex vector $\boldsymbol{V}_{V1}$ can be selected, as the blue solid arrow shown in Fig. 2. Then the origin of the reference vector is shifted to the vertex of the

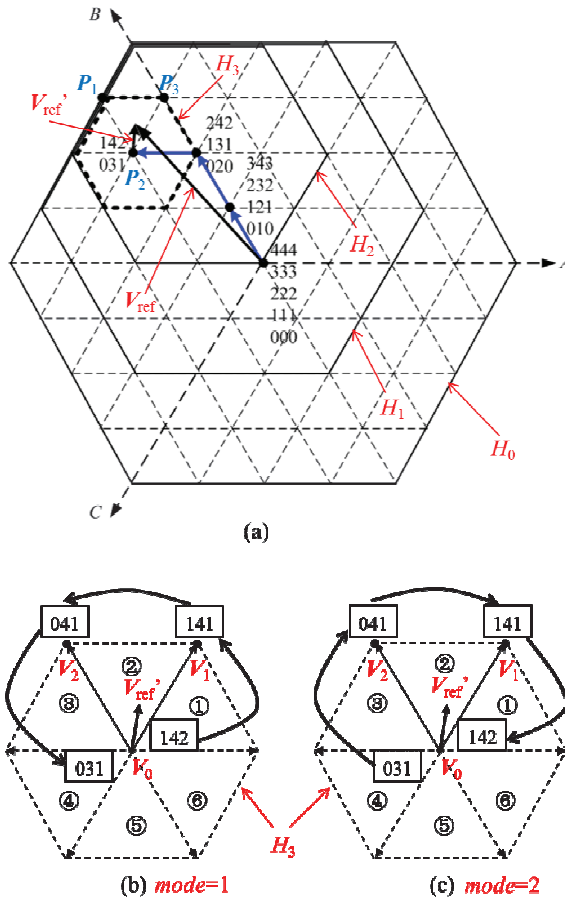


Fig. 1. SVPWM in the paper: (a) Locating the reference vector; (b)-(c) Two switching sequence modes.

selected vertex vector, which is the center vertex of the selected nested hexagon H_1, and a new reference vector $\boldsymbol{V}_{\mathrm{ref}(1)}$ is yielded. The other nested hexagons and vertex vectors can be selected in a similar way by repeating the processing in Fig. 2 based on the new reference vector.

After the set of vertex vectors is obtained, determine iteratively the switching states at the vertices (i.e., centers of the nested hexagons) for each vertex vector in the set, starting from the switching states of the inverter at the origin vertex, by modifying (increase or decrease by 1) a corresponding phase of the present switching states to produce the switching states of the inverter at the first vertex (P_2 in Fig. 1) of the modulation triangle. The type of the modification for the switching states and the corresponding phase are shown in Table I, which is called the "first mapping" and is explained in more detail in [6]. For each iteration, the type of the modification and the corresponding phase are determined based on a function s of the angle φ ($0 \le \varphi < 2\pi$) of the corresponding vertex vector

$$s = 3\varphi/\pi + 1 \tag{2}$$

Based on the first mapping in Table I, the switching states at the vertices of the vertex vectors (the centers of the nested hexagons) and the first vertex of the modulation triangle are shown in Fig. 1 and Fig. 3. The redundant switching states at each vertex are listed decreasingly from top to bottom corresponding to the switching states of phase A. The invalid switching states 454, 353, and -120 are excluded sequentially, as shown in Fig. 3.

Finally, based on the switching states obtained at the first vertex of the modulation triangle, determine the switching sequences according to the switching sequence mode (*mode*) and the region number (*reg*) of the modulation triangle in the nested 2-level hexagon H_3 as shown in Fig. 1(b)-(c). The rule of determining the switching sequence, called the "second mapping", is shown in Table II and more thoroughly explained in [6]. Correspondingly, the switching sequences according to different switching sequence modes are 142 → 141 → 041 → 031 (*mode*=1) and 031 → 041 → 141 → 142 (*mode*=2), as shown in Fig. 1(b)-(c).

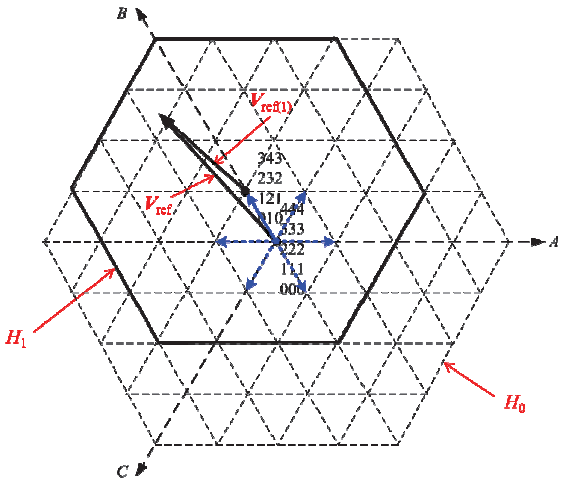


Fig. 2. Selection of the vertex vectors and nested hexagons

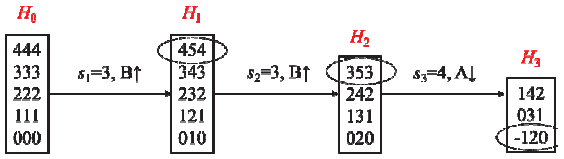


Fig. 3. Switching states at the first vertex of the modulation triangle and the vertex vectors

B. Calculation of the Duty Cycles

Based on the remainder vector $\boldsymbol{V}_{\mathrm{ref}}'$, as shown in Fig. 1(b)-(c), the duty cycles of the "nearest three vectors" are determined as for a two-level SVPWM, thus independent of the level number of the inverter. $\boldsymbol{V}_0$, $\boldsymbol{V}_1$, and $\boldsymbol{V}_2$ are

TABLE I. RULE OF THE MODIFICATION OF SWITCHING STATES (FIRST MAPPING)

s	1	2	3	4	5	6
Modification	A↑	C↓	B↑	A↓	C↑	B↓
Switching state $S_aS_bS_c$ after modification	$(S_a+1)S_bS_c$	$S_aS_b(S_c-1)$	$S_a(S_b+1)S_c$	$(S_a-1)S_bS_c$	$S_aS_b(S_c+1)$	$S_a(S_b-1)S_c$

TABLE II. RULE OF THE DETERMINATION OF SWITCHING SEQUENCES (SECOND MAPPING)

	reg					
	1	2	3	4	5	6
mode=1	ABC↑(L)	CAB↓(U)	BCA↑(L)	ABC↓(U)	CAB↑(L)	BCA↓(U)
mode=2	CBA↓(U)	BAC↑(L)	ACB↓(U)	CBA↑(L)	BAC↓(U)	ACB↑(L)

respectively equivalent to the nearest three vectors $\boldsymbol{V}_{n2}$, $\boldsymbol{V}_{n3}$, and $\boldsymbol{V}_{n1}$ in (1b).

Equation (1b) is now expressed as

$$T_s \cdot \boldsymbol{V}'_{ref} = V_{dc} \cdot (T_1 \cdot e^{j(reg-1)\pi/3} + T_2 \cdot e^{j \cdot reg \cdot \pi/3}) \quad (3)$$

where V_{dc} is voltage of the DC source of the inverter; T_1 and T_2 are respectively the duty cycle times of $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$; reg is the region number (①-⑥) of the modulation triangle in the nested 2-level hexagon H_3 as shown in Fig. 1(b)-(c).

Finally, the duty cycles are yielded from (3) as

$$\begin{cases} T_1 = \frac{2}{\sqrt{3}}[V_{rx}\, sin\left(\frac{reg}{3}\pi\right) - V_{ry}\, cos\left(\frac{reg}{3}\pi\right)] \cdot T_s \\ T_2 = -\frac{2}{\sqrt{3}}[V_{rx}\, sin\left(\frac{reg-1}{3}\pi\right) - V_{ry}\, cos\left(\frac{reg-1}{3}\pi\right)] \cdot T_s \\ T_0 = T_s - T_1 - T_2 \end{cases} \quad (4)$$

where V_{rx} and V_{ry} represent the real and imaginary part of $\boldsymbol{V}_{ref}'/V_{dc}$, respectively; T_0 is the total duty cycle for the vectors from the center vertex of the n-level hexagon H_0 to the center vertex of the nested 2-level hexagon H_3, or called the "zero vectors".

In the SVPWM scheme, two switching states (e.g., 142 and 031 in Fig. 1(b)-(c)) at the center vertex of the nested 2-level hexagon are used, and each switching state represents a "zero vector". The duty cycles T_{01} and T_{02} of the two zero vectors can be freely adjusted as long as the following equation is met

$$T_{02} = T_0 - T_{01}, \quad 0 \le T_{01} \le T_0 \quad (5)$$

C. Development of the SVPWM Scheme

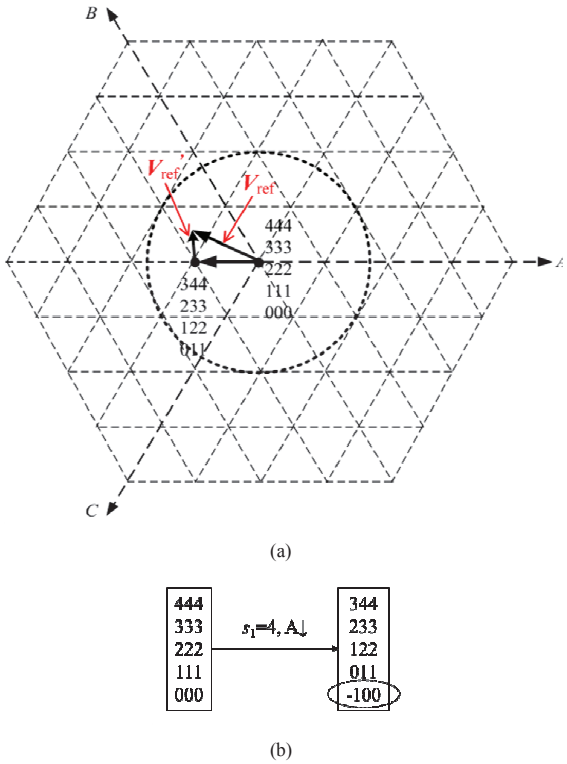
For an n-level inverter, (n-2) vertex vectors need to be generated in order to locate every reference vector, according to the locating method in Fig. 1(a). However, when the reference vector $\boldsymbol{V}_{ref}$ is in a low-modulation region, the locating processing can be simplified, as shown in Fig. 4, which is implemented as follows.

At first, classify the modulation region of the reference vector as

$$r = \text{int}\left(\frac{\|\boldsymbol{V}_{ref}\|}{\frac{\sqrt{3}}{2}V_{dc}}\right) + 1 \quad (6)$$

where int(x) means the integer part of x, and $\|\boldsymbol{V}_{ref}\|$ is the magnitude of the reference vector $\boldsymbol{V}_{ref}$ calculated from (1a).

When 1<r<n-1, the reference vector is locating in a low-modulation region, and can be treated as in a (r+1)-level space vector diagram instead of in a n-level space vector diagram, which is very useful when the level number of the inverter is high while the modulation index of the reference vector is low because less vertex vectors need to be determined.



(a)

(b)

Fig. 4. A reference vector with low modulation index: (a) Locating the reference vector; (b) Calculating the switching states.

For example, Fig. 4 shows the calculation of switching states for the reference vector $\boldsymbol{V}_{ref}$ with a relatively low modulation index (r=2 from (6)). Three vertex vectors need to be produced without classifying the modulation region in (6), while only one vertex vector is produced after the classification as shown in Fig. 4. Because of the classification in (6), when the reference vector is in the low-modulation regions, fewer vertex vectors, from (n-2) to (r-1), need to be determined, which makes the SVPWM scheme more efficient, especially when r is much smaller than n.

III. Performance Evaluation of Multilevel Inverters

In this section, the SVPWM scheme introduced in Section II is applied to analyze the performance of multilevel inverters for different influencing factors, such as switching frequency, level number of the inverter, modulation index, and switching pattern. A base operating condition of a multilevel inverter is selected as: 1) Switching frequency: 5 kHz; 2) Level number of the inverter: 9; 3) Modulation index: 0.8; and 4) Fundamental frequency: 50 Hz.

The total harmonic distortion (THD) of the output line voltage of the inverter determines the power quality supplied by the inverter and thus is considered as an evaluation

criteria for the performance of the inverter. In this paper, the THD is calculated as

$$THD = \frac{\sqrt{\|V_o\|^2 - \|V_{o1}\|^2}}{\|V_{o1}\|} \quad (7)$$

where V_o is the output line voltage of the inverter, V_{o1} is the fundamental frequency component of V_o, and $\|x\|$ represents the root mean square value of x.

The influence of each factor is described as follows.

A. Switching Frequency

Adjust the switching frequency (f_s) of the inverter from 500 Hz to 12.5 kHz (step size: 0.5 kHz) and keep the other configurations of the inverter unchanged as for the base operating condition; then the THD of the output line voltage V_{ab} (phase A to phase B) of the inverter is shown in Fig. 5. For instance, the waveforms of V_{ab} when f_s is 1 kHz, 5 kHz, and 10 kHz are respectively shown in Fig. 6.

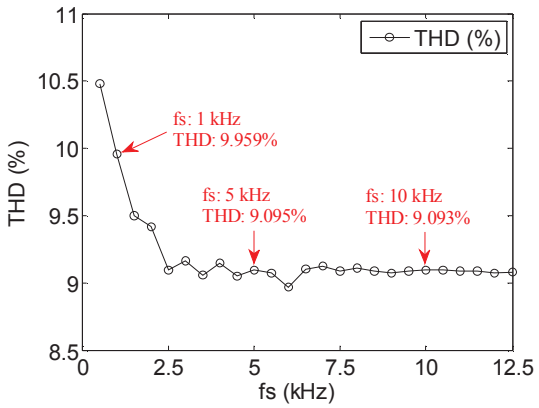


Fig. 5. THD of the inverter according to different switching frequencies

Fig. 5 reveals that for the SVPWM controlled multilevel inverter, the THD of the output line voltage is significantly reduced when the switching frequency increases until reaching a certain amount, e.g., 2.5 kHz as shown in Fig. 5. When the switching frequency is higher than about 2.5 kHz, the THD of the output line voltage does not decrease much further by simply increasing the switching frequency beyond 2.5 kHz.

Meanwhile, despite reducing THD of the output line voltage, when the switching frequency becomes higher, the power losses of the inverter will increase. So there is a compromise between the THD and power losses of the inverter, and the SVPWM scheme introduced in this paper can help to select the optimal switching frequency.

B. Level number of the Inverter

The level number of the inverter is now adjusted from 2 to 27 while keeping the other configurations of the inverter unchanged as for the base operating condition. The THD of the output line voltage V_{ab} of the inverter is shown in Fig. 8. The actual waveforms of V_{ab} when the level number of the inverter is 3, 15, and 27 for example are respectively shown in Fig. 7.

Fig. 8 illustrates that the THD of the output line voltage

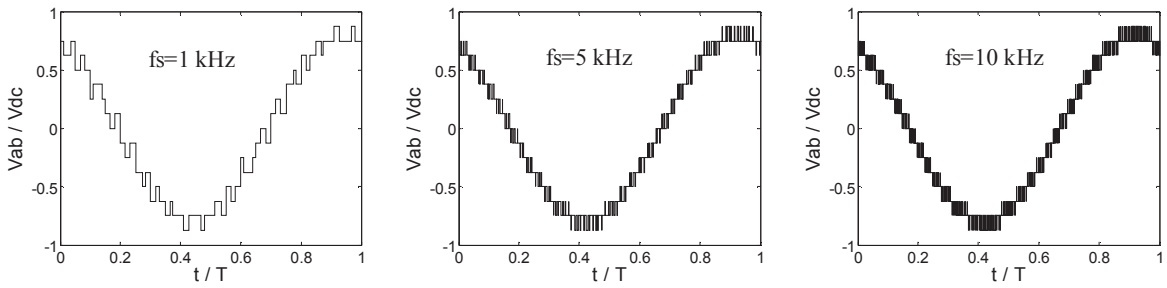


Fig. 6. Normalized PWM waveforms of the output line voltage according to different switching frequencies

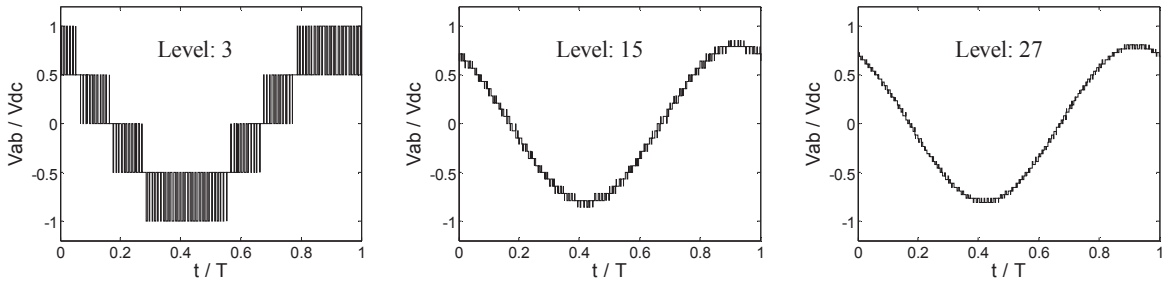


Fig. 7. Normalized PWM waveforms of the output line voltage according to different inverter levels

decreases significantly initially as the level number of the inverter increases but after about an 11-level inverter there is not much further improvement for higher levels. By comparing to Fig. 5, it also shows that when the THD of the output line voltage cannot be reduced much further by increasing the switching frequency, it can be reduced by increasing the level number of the inverter.

C. Modulation Index

Now the modulation index of the inverter is adjusted from 0.1 to 1.0 while keeping the other configurations of the inverter as the same as for the base operating condition. The THD of the output line voltage V_{ab} of the inverter now appears in Fig. 9. The actual waveforms of V_{ab} when the modulation index is 0.2, 0.5, and 1.0 are respectively shown in Fig. 10 for instance.

Fig. 9 demonstrates that the THD of the output line voltage decreases significantly when the modulation index starts increasing form a low value. However, when the modulation index is low, there are more redundant switching sequences available, which is beneficial for dc-link capacitor voltage balancing control for clamped multilevel inverters as described in [7]. The SVPWM scheme introduced in this paper can be used to select the optimal modulation index in any particular applications.

D. Switching Pattern

In the above sections, the duty cycles T_{01} and T_{02} of the two zero vectors in (5) are all selected as

$$T_{01} = T_{02} = T_0/2 \tag{8}$$

Fig. 11 shows the output voltage of phase A when the duty cycles of the zero vectors are selected as other values. When the modulation index is 0.8, there are two redundant switching sequences for each switching sequence mode according to Table II, and the output voltage of phase A for different redundant switching sequences is shown in Fig. 12.

Though the zero vectors, or redundant switching sequences, have the same effect on the output line voltage, they have different effects on the common-mode voltage brought by the inverters, and on the dc-link capacitor voltage balancing for clamped multilevel inverters [7]. Applying the SVPWM scheme described in this paper can help the inverter

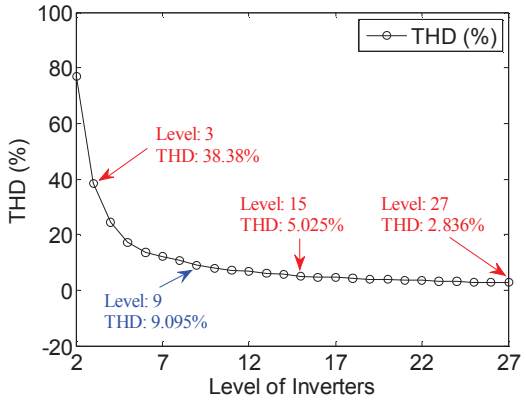


Fig. 8. THD of the inverter according to different inverter levels

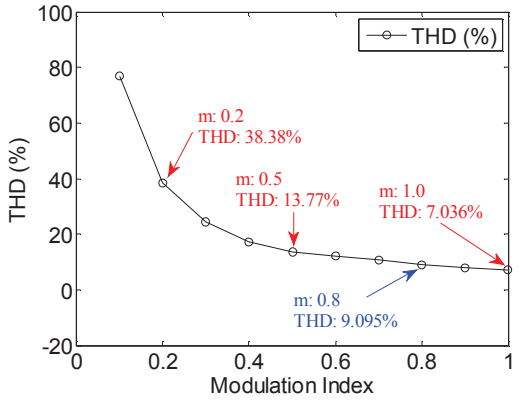


Fig. 9. THD of the inverter according to different modulation indexes

to achieve the optimal performance for any particular operating conditions/requirements.

IV. CONCLUSIONS

This paper introduces and develops a fast and generalized SVPWM scheme for multilevel inverters. Due to the development in this paper, the introduced SVPWM scheme is more efficient when the commanded reference vector is in

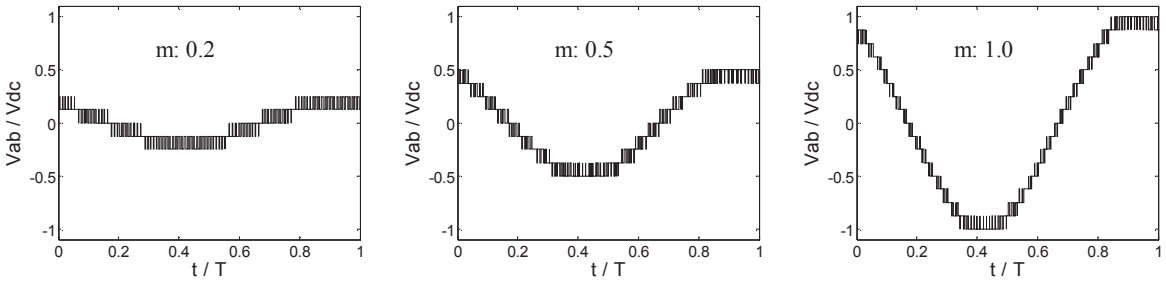


Fig. 10. Normalized PWM waveforms of the output line voltage according to different modulation indexes

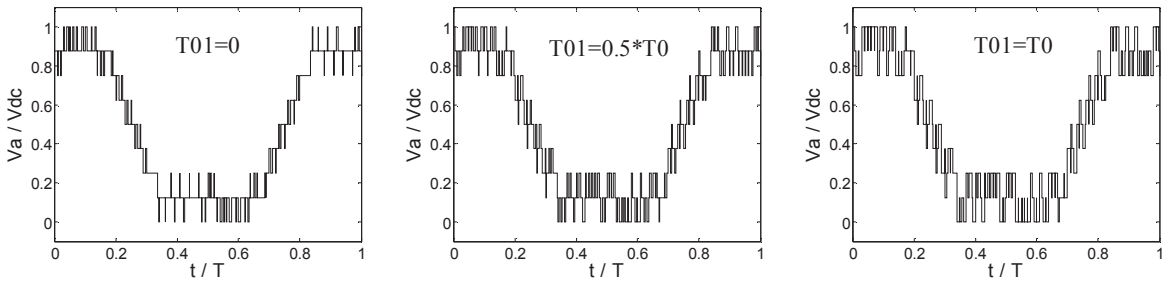


Fig. 11. Normalized PWM voltage waveforms of phase A according to different zero vector duty cycles

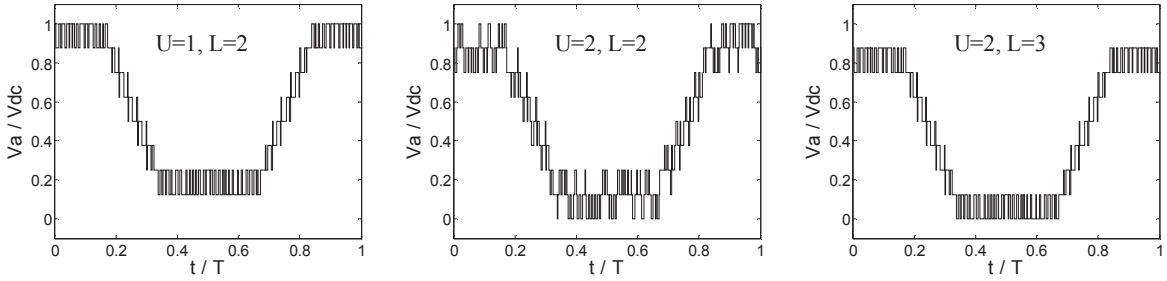


Fig. 12. Normalized PWM voltage waveforms of phase A for different redundant switching sequences

low-modulation regions. The SVPWM scheme has the following significant advantages compared with prior SVPWM schemes: 1) Switching states, duty cycles, and switching sequences are all obtained by simple calculation, so no lookup table is needed and the scheme is computationally fast; 2) All the available switching states and switching sequences can be obtained, which provides the most flexibility of optimizing switching sequence; 3) The scheme is suitable for any level inverter.

Based on the SVPWM scheme introduced in this paper, the performance of multilevel inverters is quantitatively analyzed according to different influencing factors, such as switching frequency, level number of the inverter, modulation index, and switching pattern. The results are useful for designing multilevel inverters, and the SVPWM scheme can be applied to explore the optimal performance of multilevel inverters for any particular operating conditions/requirements.

REFERENCES

[1] H. Zhang, A. Jouanne, et al., "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645-1653, Nov./Dec. 2000.

[2] J. Seo, C. Choi, and D. Hyun, "A new simplified space-vector PWM method for three-level inverters," *IEEE Trans. Power Electronics*, vol. 16, no. 4, pp. 545- 550, Jul 2001.

[3] N. Celanovic, D. Boroyevich, "A fast space vector modulation algorithm for multilevel three phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637-641, Mar./Apr. 2001.

[4] A. Gupta, A. Khambadkone, "A space vector PWM scheme for multilevel inverters based on two-level space vector PWM," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1631-1639, Oct. 2006.

[5] A. Dey, P. Rajeevan, R. Ramchand, K. Mathew, and K. Gopakumar, "A Space-Vector-Based Hysteresis Current Controller for a General *n*-Level Inverter-Fed Drive With Nearly Constant Switching Frequency Control," *IEEE Trans. Ind. Electron.*, vol. 60, no. 5, pp. 1989-1998, May 2013.

[6] Y. Deng, K. H. Teo, and R. G. Harley, "A Fast and Generalized Space Vector Modulation Scheme for Multilevel Inverters," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2013, pp. 1239-1243.

[7] Y. Deng, K. H. Teo, and R. G. Harley, "Generalized DC-Link Voltage Balancing Control Method for Multilevel Inverters," *IEEE Applied Power Electronics Conference and Exposition (APEC)*, March 2013, pp. 1219-1225.