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TR2013-131 December 2013

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*IEEE Transactions on Power Electronics*

# A Fast and Generalized Space Vector Modulation Scheme for Multilevel Inverters

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***Abstract*—This paper presents a fast and generalized space vector pulse width modulation (SVPWM) scheme for any multilevel inverter. The SVPWM scheme generates all the available switching states and switching sequences based on two simple and general mappings, and calculates the duty cycles simply as if for a two-level SVPWM, thus independent of the level number of the inverter. Because the switching states, duty cycles, and switching sequences are all obtained by simple calculation in the proposed SVPWM scheme, no lookup table is needed and the scheme is computationally fast. The generalized method of generating the switching states (first mapping), calculating the duty cycles, and determining the switching sequence (second mapping) is described in the paper. The scheme is suitable for any reference vector with any modulation index, and can be conveniently extended to meet specific requirements, such as symmetric switching sequences. Compared with prior methods, the SVPWM scheme proposed in this paper provides two more degrees of freedom, i.e., the adjustable switching sequences and duty cycles, thus offering significant flexibility for optimizing the performance of multilevel inverters. The influence of redundant switching sequences in the output phase voltage of inverters is demonstrated for a nine-level inverter. This paper also thoroughly compares the proposed SVPWM scheme with prior methods. Both simulation and experimental results are given.**

***Index Terms*—Adjustable duty cycles, multilevel inverter, redundant switching sequences, space vector modulation, SVPWM**

## I. Introduction

MULTILEVEL inverters are widely used in high-power high-voltage applications due to their advantageous performance compared to two-level inverters, including reduced voltage stress on the power devices, lower harmonics, lower instantaneous rate of voltage change ($dv/dt$), and lower common-mode voltage [1]-[7]. Multilevel inverters have recently been shown to be even more promising due to the emerging technology called modular multilevel converters [8]-[10]. Among various modulation strategies for multilevel inverters, space vector pulse width modulation (SVPWM), also called space vector modulation (SVM), attracts much attention because it provides significant flexibility to optimize switching waveforms, and is suitable for implementation in digital signal processors [11]. A general diagram of a SVPWM based clamped $n$-level inverter is shown in Fig. 1. However, in spite of its significant advantages, SVPWM for more than three-level inverters is still hardly explored, due to the largely increased number of switching states and switching sequences that accompany the higher number of levels. Generally, for an $n$-level inverter, there are $n^3$ switching states and $6(n\text{-}1)^2$ triangles in the space vector diagram [12].

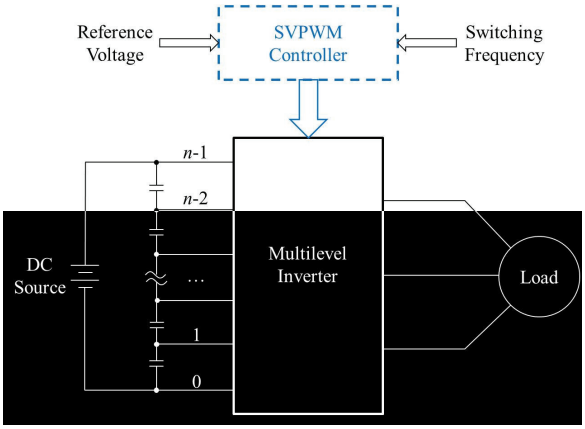


Fig. 1. Block diagram of a multilevel inverter

Several SVPWM schemes [11]-[15] are known for three-level inverters. Due to some drawbacks, however, those schemes are not readily extended to four or higher level inverters. Moreover, most of those schemes focus on calculating the duty cycles, but in fact the determination of all redundant switching states and appropriate switching sequence is more challenging for SVPWM schemes. A Euclidean vector system based SVPWM algorithm is presented in [11]. However, several matrix transformations are needed, and no systematic approach for determining the switching sequences or real-time implementation is provided. The loss of effectiveness in over-modulation regions is another challenge for the method in [11]. A coordinate transformation and switching sequence

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mapping based SVPWM scheme is proposed in [12], in which a coordinate transformation is needed to determine the location of the reference vector and to calculate the duty cycles, and a pre-stored switching sequence mapping table is needed to determine the switching sequence. Since the number of possible switching sequences increases sensitively with the increasing level number of the inverter, more memory will be needed and slower mapping speed will be achieved when the method in [12] is applied to higher level inverters.

One method partitions the three-level space vector diagram into six two-level space vector diagrams [13]. However, the axes of the *d*-*q* plane need to be rotated by a certain angle in each calculation of the reference vector location and thus the method is not easily applied to higher level inverters; and no general method for switching sequence selection or application for four or higher level inverter is introduced. A similar method for three-level inverters is described in [14], in which a two-phase to three-phase conversion is needed to calculate the shift of origin of a virtual two-level inverter. Since the two-phase to three-phase conversion is needed for each division of the space vector diagram, both the complexity and computation of this scheme will increase when applied to a four or higher level inverter. Moreover, no general switching sequence selection method is introduced either. In [15], the equivalent two-level sub-hexagon is detected, which contains the tip of the reference vector in the space vector diagram of the multilevel inverter, and then the origin of the reference vector is relocated to the center of the two-level sub-hexagon. However, some switching states and switching sequences that are actually suitable for the reference vector are ignored in this method, which causes the method to not provide optimal switching waveforms for every operation condition.

This paper proposes a new SVPWM scheme for multilevel inverters that overcomes the above drawbacks and generates all the available switching states and switching sequences based on two simple and general mappings. Moreover, it calculates the duty cycles simply as if it were an equivalent two-level SVPWM, thus independent of the level number of the inverter. This new SVPWM scheme has the following salient features:

1) Switching states, duty cycles, and switching sequences are all obtained by simple calculation, thus no lookup table is required, less memory is needed, and the scheme is computationally fast.

2) Compared with earlier methods, the SVPWM scheme proposed in this paper provides two more degrees of freedom, i.e., the adjustable switching sequences and duty cycles.

3) All the available switching states and switching sequences are obtained, which provides the most flexibility for optimizing switching sequences.

4) The scheme works well for any reference vector with any modulation index, and can be conveniently extended to meet specific requirements, e.g., symmetric switching sequences.

5) The scheme is suitable for any level of inverter.

The rest of the paper is organized as follows: Section II describes the principle of the SVPWM scheme in detail, including locating the reference vector, calculating the duty cycles, and generating the switching sequences; Section III introduces several extensions of the proposed SVPWM scheme and compares the proposed SVPWM scheme with typical earlier methods; Section IV presents the experimental results of a 101-level inverter; and Section V concludes the paper.

## II. Basic Principle of the SVPWM Scheme

For an *n*-level inverter shown in Fig. 1, the output voltage vector in this paper is defined as [16]

$$\boldsymbol{V}_{out} = V_{dc} \cdot (S_a + S_b \cdot e^{j\frac{2}{3}\pi} + S_c \cdot e^{j\frac{4}{3}\pi}) \tag{1}$$

where $V_{dc}$ is voltage of the DC source, and $S_a$, $S_b$, and $S_c$ are the switching states of phase A, B, and C, respectively. If the values of $S_a$, $S_b$ and $S_c$ are defined as $S_a$, $S_b$, $S_c$=0, 1, …$n$-1, then the output voltages of phases A, B, and C relative to the negative terminal of the DC source are $S_a \cdot V_{dc}/(n\text{-}1)$, $S_b \cdot V_{dc}/(n\text{-}1)$, and $S_c \cdot V_{dc}/(n\text{-}1)$, respectively. When the $n$-level inverter is a cascaded inverter [2], the definition in (1) is still suitable, and in this situation $V_{dc}/(n\text{-}1)$ represents the smallest voltage among the separate DC sources.

A space vector diagram containing all the output vectors and the corresponding switching states of the inverter, can be generated based on (1), e.g., Fig. 2 shows the space vector diagram of a five-level inverter calculated in this way. In the space vector diagram, the number at each vertex represents the switching state $S_aS_bS_c$ of the inverter, where $S_a$, $S_b$, and $S_c$ are respectively the switching states of phase A, B, and C as in (1). For example, the number 041 at vertex $P_1$ means that for the vector $\boldsymbol{OP}_1$, the corresponding switching states of phase A, B, and C are $S_a$=0, $S_b$=4, and $S_c$=1. Some vectors can be equivalently produced by more than one switching state of the inverter, and those switching states at the vertex of the vector are listed decreasingly from top to bottom corresponding to the switching states of phase A in the space vector diagram. For example, the numbers 344, 233, 122, and 011 are all valid switching states for generating the vector with tip $P_4$, and they are listed decreasingly from top to bottom corresponding to the switching states of phase A.

A reference vector $\boldsymbol{V}_{ref}$ and the corresponding "nearest three vectors" $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$ are also shown in Fig. 2. The vertices of the nearest three vectors compose a so called "modulation triangle", which encloses the reference vector. In order to synthesize or equate the reference vector, it is the task of the SVPWM scheme to detect the nearest three vectors (i.e., the switching states of the vertices $P_1$, $P_2$, and $P_3$), to determine the sequence of the nearest three vectors during a switching cycle (i.e., the switching sequence), and to calculate the needed on-time (i.e., duty cycle) of each nearest vector based on the following equation [11]

$$T_s \cdot \boldsymbol{V}_{ref} = d_1 \cdot \boldsymbol{OP}_1 + d_2 \cdot \boldsymbol{OP}_2 + d_3 \cdot \boldsymbol{OP}_3 \tag{2}$$

where $T_s$ is the commanded switching cycle, and $d_1$, $d_2$, and $d_3$ are the duty cycle periods of $\boldsymbol{OP}_1$, $\boldsymbol{OP}_2$, and $\boldsymbol{OP}_3$, respectively.

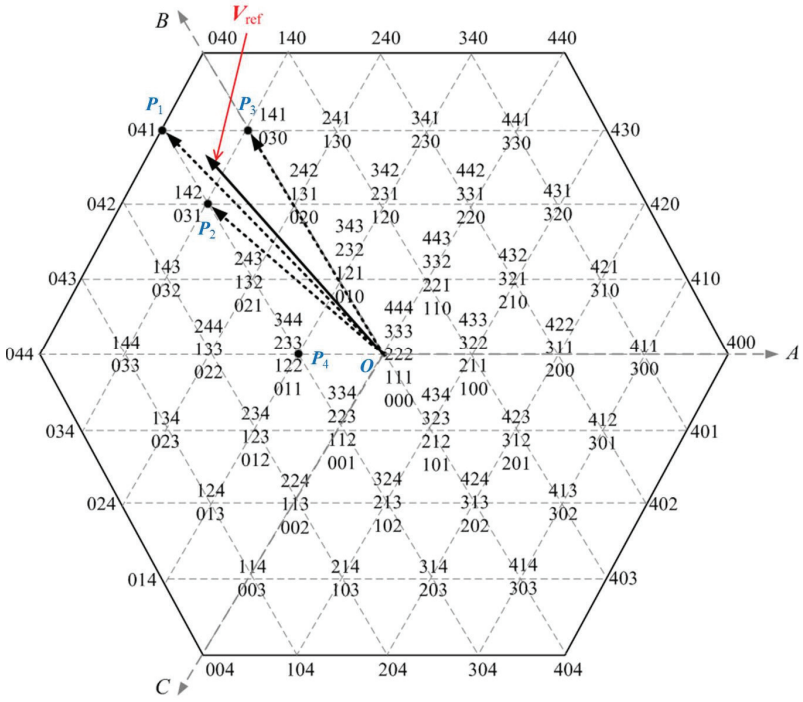



Fig. 2. Space vector diagram of a five-level inverter

The SVPWM scheme proposed in this paper is illustrated in Fig. 3 [17]. Fig. 3(a) shows how to locate the reference vector (i.e., to detect the modulation triangle $\Delta P_1P_2P_3$); Fig. 3(b)-(c) show how to calculate the duty cycles and to generate the switching sequences in two modes, i.e., counterclockwise (*mode*=1) and clockwise (*mode*=2), as if it were an equivalent two-level SVPWM. In Fig. 3(b)-(c), $\boldsymbol{V}_0$, $\boldsymbol{V}_1$, and $\boldsymbol{V}_2$ are respectively equivalent to the nearest three vectors $\boldsymbol{OP}_2$, $\boldsymbol{OP}_3$, and $\boldsymbol{OP}_1$. Fig. 3 is described below in more detail. For purposes of demonstration, the proposed SVPWM illustration is based on the space vector diagram of a five-level inverter shown in Fig. 2. It is understood that the SVPWM scheme can be implemented in any level of inverter.

### *A. Locating the Reference Vector*

First, the reference vector $\boldsymbol{V}_{ref}$ is represented as the sum of a set of "vertex vectors" ($\boldsymbol{OO}_1$, $\boldsymbol{O}_1\boldsymbol{O}_2$, and $\boldsymbol{O}_2\boldsymbol{P}_2$) and a "remainder vector" $\boldsymbol{V}_{ref}'$, as shown in Fig. 3(a). A vertex vector is a vector connecting two adjacent vertices. The vertex vectors connect the center vertex of the *n*-level space-vector diagram $H_0$ with a first vertex (i.e., $P_2$) of the modulation triangle ($\Delta P_1P_2P_3$) enclosing the reference vector. The remainder vector is the vector enclosed by the modulation triangle and connecting the first vertex of the modulation triangle with the reference vector.

One way to determine the set of vertex vectors is based on determining a set of nested hexagons $H_1$, $H_2$, and $H_3$ enclosing the reference vector, as shown in Fig. 3(a). Each nested hexagon corresponds to a specific level ranging from (*n*-1) to a second level, and centers at the vertex of a vertex vector. For instance, the method of selecting the nested (*n*-1)-level hexagon $H_1$ is shown in Fig. 4. The other nested hexagons can be selected in a similar way.

As shown in Fig. 4(a), the *n*-level space-vector diagram $H_0$ is partitioned into six sectors by six dashed lines. The six dashed lines pass through the center of the *n*-level space-vector diagram and their angles are from $\pi/6$ to $11\pi/6$, and the angle between any two adjacent dashed lines is $\pi/3$. Then consider the *n*-level space-vector diagram as being composed of six hexagons that are the space-vector diagrams of (*n*-1)-level inverters, and whose center vertices ($O_1$, and $Q_1$ - $Q_5$) compose a 2-level hexagon enclosing the center of $H_0$. For clarity, only three hexagons $SH_1$, $SH_2$, and $SH_3$ of the six (*n*-1)-level space-vector hexagons are shown in Fig. 4(a), and the other three (*n*-1)-level hexagons can be reached by shifting the center of $SH_1$ to the corresponding centers of the (*n*-1)-level hexagons. Consequently, the nested (*n*-1)-level hexagon $H_1$ is selected as the one whose center locates in the same sector as the reference vector does (i.e., $SH_3$), which in Fig. 4(a) means that the angle $\theta_0$ of the reference vector has values within the following range

$$\pi/2 \le \theta_0 < 5\pi/6 \tag{3}$$

The first vertex vector $\boldsymbol{V}_{V1}$ is thus the vector that connects the center vertices of $H_0$ and $H_1$, as shown in Fig. 4(a).

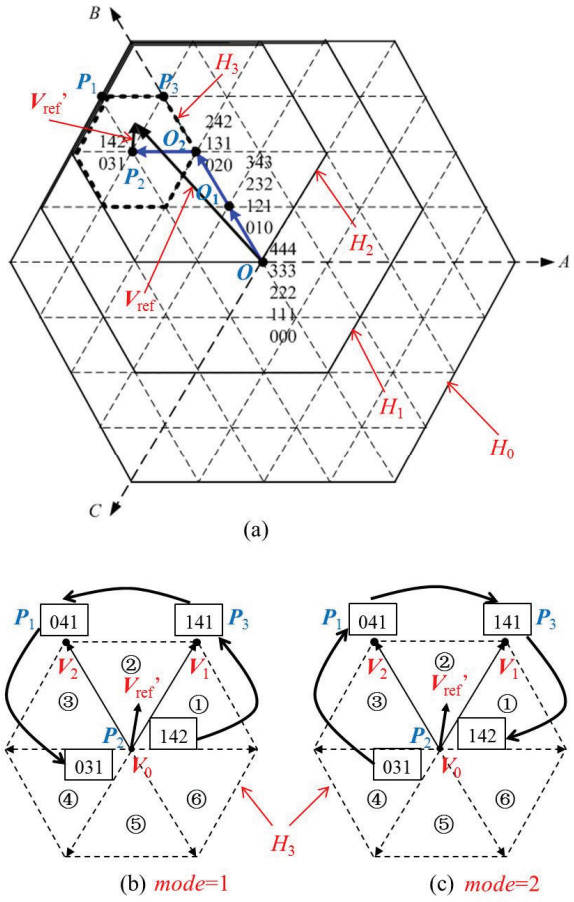



Fig. 3. SVPWM proposed in the paper: (a) Locating the reference vector; (b)-(c) Two switching sequence modes.

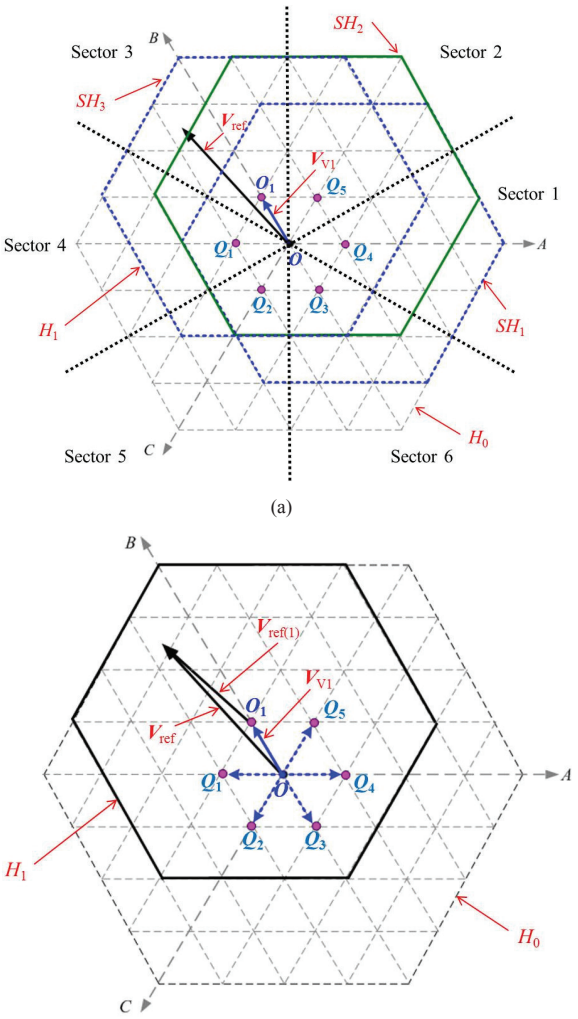



Fig. 4. Selection of the nested hexagons: (a) Division of the space vector diagram; (b) First center vertex.

Another equivalent way to determine the vertex vectors is shown in Fig. 4(b). There are six vertex vectors available for the nested ($n$-1)-level hexagon $H_1$, i.e., the one blue solid arrow ($\boldsymbol{OO}_1$) and five blue dashed arrows ($\boldsymbol{OQ}_1$ - $\boldsymbol{OQ}_5$) as shown in Fig. 4(b). The actual vertex vector, among the six available vertex vectors, for the nested ($n$-1)-level hexagon $H_1$, is the one for which the angle between this vertex vector and the reference vector is the smallest. In this way, the first vertex vector $\boldsymbol{V}_{V1}$ can also be selected, as shown in Fig. 4(b).

Generally, the angle ($\varphi_1$) of the first vertex vector are determined by the angle $\theta_0$ ($0 \le \theta_0 < 2\pi$) of the reference vector as

$$\varphi_1 = \mathrm{int}\left\{\mathrm{mod}\left(\theta_0 + \frac{\pi}{6}, 2\pi\right) \cdot \frac{3}{\pi}\right\} \cdot \pi/3 \tag{4}$$

where the function int($x$) means the integer part of $x$, and the function mod($x$, $y$) represents the remainder of $x$ divided by $y$. After the first vertex vector is determined, the origin of the reference vector $\boldsymbol{V}_{ref}$ is shifted to the center vertex of $H_1$, which yields a new reference vector $\boldsymbol{V}_{ref(1)}$ as

$$\boldsymbol{V}_{ref(1)} = \boldsymbol{V}_{ref} - V_{dc} \cdot e^{j\varphi_1} \tag{5}$$

Based on $\boldsymbol{V}_{ref(1)}$, all the other nested hexagons and vertex vectors can be determined by repeating the processing shown in Fig. 4 and the calculation in (4) and (5).

After the set of vertex vectors is obtained, determine iteratively the switching states at the vertices (i.e., centers of the nested hexagons) for each vertex vector in the set of vertex vectors, starting from the present switching states of the inverter at the origin vertex, by modifying (increase or decrease by 1) a corresponding phase of the present switching states to produce the switching states of the inverter at the first vertex ($P_2$ in Fig. 3) of the modulation triangle. The type of the modification for the switching states and the corresponding phase are shown in Table I, which is called the "first mapping" in this paper and will be explained later. For each iteration, the

TABLE I

RULE OF THE MODIFICATION OF SWITCHING STATES (FIRST MAPPING)

| $s$ | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| Modification | A↑ | C↓ | B↑ | A↓ | C↑ | B↓ |
| Switching state $S_aS_bS_c$ after modification | $(S_a+1)S_bS_c$ | $S_aS_b(S_c-1)$ | $S_a(S_b+1)S_c$ | $(S_a-1)S_bS_c$ | $S_aS_b(S_c+1)$ | $S_a(S_b-1)S_c$ |

type of the modification and the corresponding phase are determined based on a function $s$ (represents the order number of the Sector containing the reference vector as in Fig. 4(a)) of the angle $\varphi$ of the corresponding vertex vector relative to axis $A$, and the function $s$ of the angle $\varphi$ ($0 \le \varphi < 2\pi$) of the corresponding vertex vector can be described as

$$s = 3\varphi/\pi + 1 \tag{6}$$

A method that obtains the function $s$ directly for each new reference vector calculated in (5) is introduced in the Appendix and avoids the inverse trigonometric computing for calculating the angle of the reference vector, and thus is more suitable for digital signal processors.

The rule of the modification for the switching states (the "first mapping") according to the function $s$ is shown in Table I, in which the letters A, B, or C means the switching state of phase A, B, or C respectively that needs to be modified. The up-arrow "↑" means the switching state of the phase needs to increase by 1, and the down-arrow "↓" means the switching state of the phase needs to decrease by 1. For example, if a switching state is $S_aS_bS_c$ and the modification rule is "A↑" ($s$=1), then the switching state after the modification is $(S_a+1)S_bS_c$. The switching states after the modification for other values of $s$ are also summarized in Table I. Since the switching states for each phase of an $n$-level inverter can only have a value from 0 to ($n$-1) by definition in this paper, a switching state needs to be excluded when the corresponding switching state of phase A, B, or C is larger than ($n$-1) or less than 0.

Based on the first mapping in Table I, the switching states at the vertices of the vertex vectors (the centers of the nested hexagons) and the first vertex of the modulation triangle are shown in Fig. 3 and Fig. 5, which can be verified by comparing it with the space vector diagram of the 5-level inverter shown in Fig. 2. The invalid switching states 454, 353, and -120 are excluded sequentially, as shown in Fig. 5. For example, for the vertex vector from the center of $H_2$ to the center of $H_3$, the value of $s$ in (6) is $s_3$=4, thus the modification rule according to Table I is "A↓". Because the switching states at the center of hexagon $H_2$ are 242, 131, and 020, the switching states at the center of hexagon $H_3$ (the first vertex $P_2$ of the modulation triangle) can be calculated as 142 and 031 (the invalid switching state -120 is removed).

The rationale for the first mapping (Table I) is based on (1). For a vertex vector, the shift of the origin of the reference vector is $V_{dc} \cdot e^{j(s-1)\pi/3}$ ($s$ is calculated in (6)), which can be

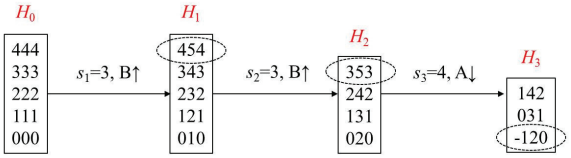
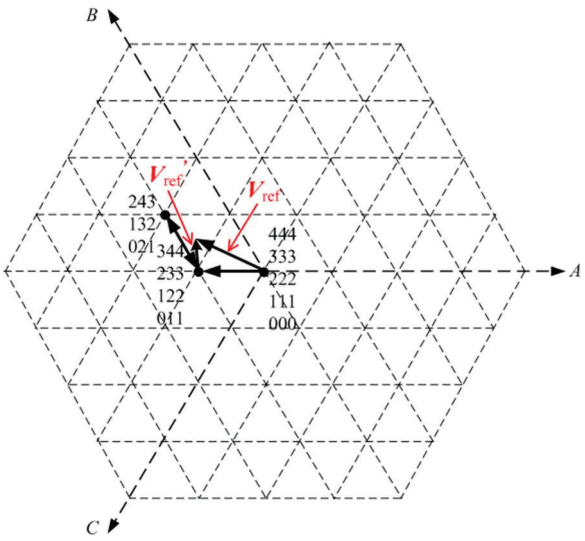
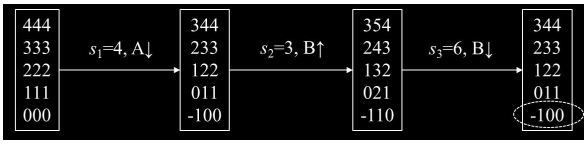



Fig. 5. Switching states at the first vertex of the modulation triangle and the vertex vectors




(a)




(b)

Fig. 6. A reference vector with a low modulation index: (a) Locating the reference vector; (b) Calculating the switching states.

substituted into (1) to determine the required modification for the present switching states of phase A, B, or C. The first mapping is suitable for any level inverter and any reference vectors with any modulation indexes. Fig. 6 shows an example when the modulation index of the reference vector is relatively low. The switching states at the first vertex of the modulation triangle are correctly calculated, but the calculation can be further simplified, which will be introduced in detail in Section III.

### B. Calculating the Duty Cycles

Based on the remainder vector $\boldsymbol{V}_{ref}'$, as shown in Fig. 3(b)-(c), the duty cycles of the "nearest three vectors" are determined as for a two-level SVPWM, thus independent of the level number of the inverter. $\boldsymbol{V}_0$, $\boldsymbol{V}_1$, and $\boldsymbol{V}_2$ are respectively equivalent to the nearest three vectors $\boldsymbol{OP}_2$, $\boldsymbol{OP}_3$, and $\boldsymbol{OP}_1$.

Equation (2) is now expressed as

$$T_s \cdot \boldsymbol{V}_{ref}' = V_{dc} \cdot (T_1 \cdot e^{j(reg-1)\pi/3} + T_2 \cdot e^{j \cdot reg \cdot \pi/3}) \quad (7)$$

where $T_s$ is the commanded switching cycle; $T_1$ and $T_2$ are respectively the duty cycle periods of $\boldsymbol{V}_1$ and $\boldsymbol{V}_2$; *reg* is the region number (①-⑥) of the modulation triangle in the nested 2-level hexagon $H_3$ as shown in Fig. 3(b)-(c), and can be calculated as

$$reg = \text{int}(3\theta_{rem}/\pi) + 1 \quad (8)$$

where $\theta_{\text{rem}}$ ($0 \le \theta_{\text{rem}} < 2\pi$) is the angle of the remainder vector, and int($3\theta_{\text{rem}}/\pi$) means the integer part of $3\theta_{\text{rem}}/\pi$. For example, *reg*=2 in Fig. 3(b)-(c). An alternative way to calculate the value of *reg* is introduced in the Appendix, which avoids the inverse trigonometric computing for the angle $\theta_{\text{rem}}$ of the remainder vector, and thus is more suitable for digital signal processors.

Finally, the duty cycles are

$$\begin{cases} T_1 = \frac{2}{\sqrt{3}}[V_{rx} \sin\left(\frac{reg}{3}\pi\right) - V_{ry} \cos\left(\frac{reg}{3}\pi\right)] \cdot T_s \\ T_2 = -\frac{2}{\sqrt{3}}[V_{rx} \sin\left(\frac{reg-1}{3}\pi\right) - V_{ry} \cos\left(\frac{reg-1}{3}\pi\right)] \cdot T_s \\ T_0 = T_s - T_1 - T_2 \end{cases} \quad (9)$$

where $V_{\text{rx}}$ and $V_{\text{ry}}$ represent the real and imaginary part of $\boldsymbol{V}_{ref}'/V_{dc}$, respectively; $T_0$ is the total duty cycle period for the vectors from the center vertex of the *n*-level hexagon $H_0$ to the center vertex of the nested 2-level hexagon $H_3$, or called the "zero vectors" in this paper.

In the SVPWM scheme, two switching states (e.g., 142 and 031 in Fig. 3) at the center vertex of the nested 2-level hexagon are used, and each switching state represents a "zero vector". The duty cycle periods $T_{01}$ and $T_{02}$ of the two zero vectors can be freely adjusted as long as the following equation is met

$$T_{02} = T_0 - T_{01}, \quad 0 \le T_{01} \le T_0 \quad (10)$$

Since different zero vectors have different influences on the voltages across the dc-link capacitors of a multilevel inverter [18] [19] and on the harmonic distortion of the flux trajectories [20], the SVPWM scheme provides more flexibility for balancing the dc-link capacitor voltages and approaching the ideal flux trajectories.

### C. Generating the Switching Sequence

Based on the switching states (i.e., 142 and 031 as in Figs. 3 and 5) obtained at a first vertex (i.e., $P_2$) of the modulation triangle, the switching sequences are determined according to the switching sequence mode (*mode*) and the region number (*reg*) of the modulation triangle in the nested 2-level hexagon $H_3$. There are two switching sequence modes in the paper, i.e., the switching sequence mode is *mode*=1 when the switching sequence is counterclockwise selected as in Fig. 3(b), and the switching sequence mode is *mode*=2 when the switching sequence is clockwise selected as in Fig. 3(c).

The rule of determining the switching sequence, called the "second mapping", is shown in Table II, in which each element of the mapping includes 5 sub-elements. The variable *reg* is the region number of the modulation triangle calculated in (8). The letter A, B, or C means the switching state of phase A, B, or C is to be modified sequentially. The symbol "↑" or "↓" means the state of the corresponding phase is increased by 1 or decreased by 1, respectively. For example, if the first switching state of a switching sequence is $S_aS_bS_c$ and the switching sequence rule is "ABC↑(L)" (i.e., *reg*=1 and *mode*=1) according to Table II, then the switching sequence is generated as $S_aS_bS_c \rightarrow (S_a+1)S_bS_c \rightarrow (S_a+1)(S_b+1)S_c \rightarrow (S_a+1)(S_b+1)(S_c+1)$. In the space vector diagram, the redundant switching states at each vertex are listed decreasingly from top to bottom corresponding to the switching states of phase A, as shown in Fig. 2. For example, the switching states 344, 233, 122, and 011 at vertex $P_4$ are listed decreasingly from top to bottom corresponding to the switching states of phase A. The letter "L" in the parentheses represents the word "lower" and means the first switching state at the first vertex of the modulation triangle should not be the top one, e.g., not 344 for vertex $P_4$; and the letter "U" in the parentheses represents the word "upper" and means the first switching state at the first vertex of the modulation triangle should not be the bottom one, e.g., not 011 for vertex $P_4$. Based on the second mapping, the switching sequences for the reference vector in Fig. 2 according to different switching sequence modes are summarized in Table III and shown in Fig. 3(b)-(c), and the accuracy of the switching sequences can be verified by comparison with the space vector diagram shown in Fig. 2.

TABLE II

RULE OF THE DETERMINATION OF SWITCHING SEQUENCES (SECOND MAPPING)

| | *reg* | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| *mode*=1 | ABC↑(L) | CAB↓(U) | BCA↑(L) | ABC↓(U) | CAB↑(L) | BCA↓(U) |
| *mode*=2 | CBA↓(U) | BAC↑(L) | ACB↓(U) | CBA↑(L) | BAC↓(U) | ACB↑(L) |

Consider "CAB↓(U)" when *reg*=2 and *mode*=1 (shown in Fig. 3(b)) as an example to explain the switching sequence selection method in this paper. Because *mode* = 1, the switching sequence is $\boldsymbol{V}_0 \rightarrow \boldsymbol{V}_1 \rightarrow \boldsymbol{V}_2 \rightarrow \boldsymbol{V}_0$. From $\boldsymbol{V}_0$ to $\boldsymbol{V}_1$, since *reg* = 2, the change of the vector is $V_{dc} \cdot e^{j\pi/3}$, which can be substituted into (1) and means that the switching state of phase C decreases by one. From $\boldsymbol{V}_1$ to $\boldsymbol{V}_2$, the change of the vector is $V_{dc} \cdot e^{j\pi}$, which can be substituted into (1) and means that the switching state of phase A decreases by one. Similarly, from $\boldsymbol{V}_2$ to $\boldsymbol{V}_0$, the change of the vector is $V_{dc} \cdot e^{j5\pi/3}$, which means the switching state of phase B decreases by one. All the switching sequences for other values of *reg* and *mode* can be analyzed in the similar way, and the rule of determining the switching sequence can be mapped as the second mapping.

The second mapping is suitable for any level inverter and any reference vectors with any modulation indexes, and can be conveniently extended to meet other specific requirements, e.g., symmetric switching sequences. For example, based on the second mapping, the switching sequences for the reference vector in Fig. 6 with a relatively low modulation index are summarized in Table IV, which shows that when the modulation index is low, more than one switching sequences are suitable for the reference vector and the SVPWM scheme can generate all of them. This will be further introduced in the next section.

Since all the redundant switching sequences can be generated based on the second mapping, the optimal switching sequences for different applications can be easily selected. The optimized switching sequences, for example, achieving minimum number of switching transitions in a fundamental cycle as described in [20] can be obtained by simply choosing the first switching state of a switching sequence as that closest to the last switching state of the previous switching sequence. Moreover, because different switching sequences have different effects on the voltages across the dc-link capacitors of a multilevel inverter [19] [21] [22], the SVPWM scheme provides more flexibility for balancing the dc-link capacitor voltages.

It should be mentioned that the second mapping in Table II is for generating the continuous switching sequences (i.e., no switching state is eliminated). The second mapping can also be conveniently modified to produce discontinuous SVPWM patterns [20] (i.e., eliminating either the first or last switching state in each switching sequence), since discontinuous SVPWM can potentially increase the switching frequency and thus provide harmonic benefits for certain modulation ranges. For example, if the discontinuous pattern DPWMMAX [20] is desired for the reference vector $\boldsymbol{V}_{\text{ref}}$ shown in Fig. 2, the modulation rule for *reg*=2 and *mode*=1 is adjusted to "CA↓(U)", and the corresponding discontinuous switching sequence is 142 → 141 → 041, which means phase B is unmodulated. The rules for other discontinuous patterns can be summarized in a similar way.

### D. Simulation Results

The simulated output voltages of phase A for five-, six-, and seven-level inverters are shown in Fig. 7, and the simulated output line voltages (phase A to phase B) for eight-, nine-, and ten-level inverters are shown in Fig. 8. In the simulation, the switching frequency is 5 kHz (fundamental frequency is 50 Hz), the modulation index of the reference vector is 0.9, the duty cycles of the two zero vectors are set as $T_{01}$=$T_{02}$=$T_0$/2 in (10), and the switching sequence mode is changed (alternately from one mode to the other) after every switching cycle.

TABLE III

SWITCHING SEQUENCES FOR DIFFERENT MODES

| | |
|---|---|
| *mode*=1 | 142 → 141 → 041 → 031 |
| *mode*=2 | 031 → 041 → 141 → 142 |

TABLE IV

SWITCHING SEQUENCES FOR DIFFERENT MODES (LOW MODULATION INDEX)

| | |
|---|---|
| *mode*=1 | 344 → 343 → 243 → 233 |
| | 233 → 232 → 132 → 122 |
| | 122 → 121 → 021 → 011 |
| *mode*=2 | 011 → 021 → 121 → 122 |
| | 122 → 132 → 232 → 233 |
| | 233 → 243 → 343 → 344 |

## III. EXTENSION OF THE SVPWM SCHEME AND COMPARISON WITH EARLIER METHODS

The basic principle of the proposed SVPWM scheme has been introduced in the above section. Now, in this section, some extensions of the SVPWM scheme are presented, which will provide the SVPWM scheme with a better performance and broader applications. The comparison between the proposed SVPWM scheme and typical earlier methods is also given.

### A. Classification of the Modulation Region

According to (1), the reference vector input to the SVPWM controller of the *n*-level inverter is

$$\boldsymbol{V}_{ref} = (n-1) \cdot \left( V_a^* + V_b^* \cdot e^{j\frac{2}{3}\pi} + V_c^* \cdot e^{j\frac{4}{3}\pi} \right)$$

$$= (n-1) \cdot \left( m \cdot \frac{\sqrt{3}}{2} V_{dc} \cdot e^{j\theta} \right) = V_m \cdot e^{j\theta} \qquad (11)$$

where $V_a^*$, $V_b^*$, and $V_c^*$ are respectively the command reference voltage of phase A, B, and C; $m$ is the modulation index; and $\theta$ is the phase angle of the phase A voltage. As shown in Fig. 9, the space vector diagram of the multilevel inverter in Fig. 2 can be divided into different regions by the circles. Each circle is an inscribed circle of a hexagon, and the hexagon represents the space vector diagram of a certain level inverter. Accordingly, the region containing the reference vector is classified or numbered as

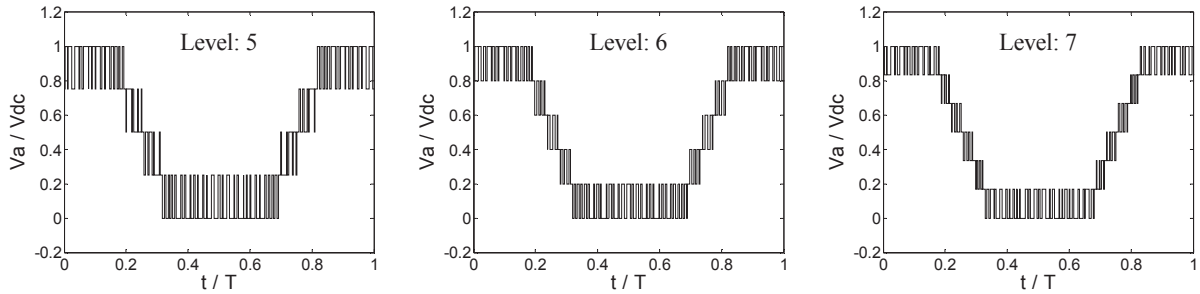



Fig. 7. Normalized PWM voltage waveforms of phase A for five-, six-, and seven-level inverters

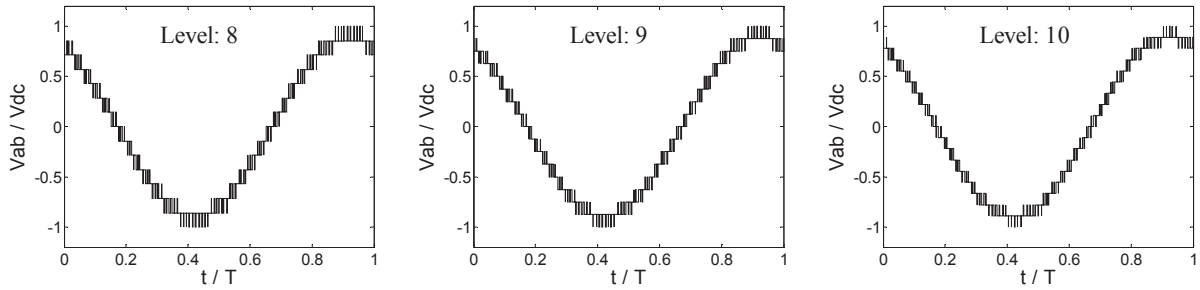



Fig. 8. Normalized PWM waveforms of the output line voltage according to different inverter levels

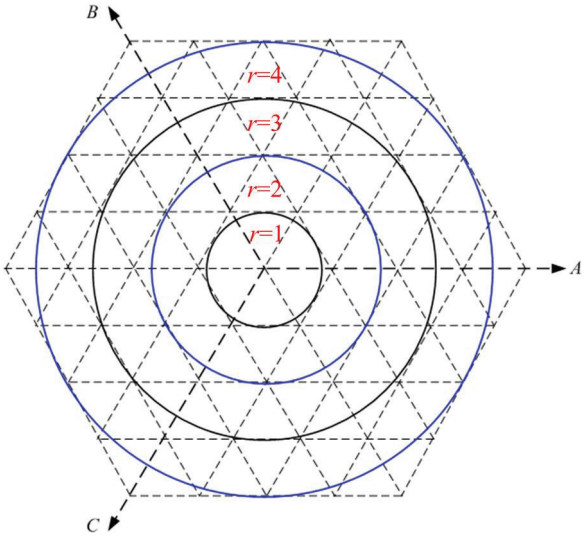



Fig. 9. Classification of the modulation region

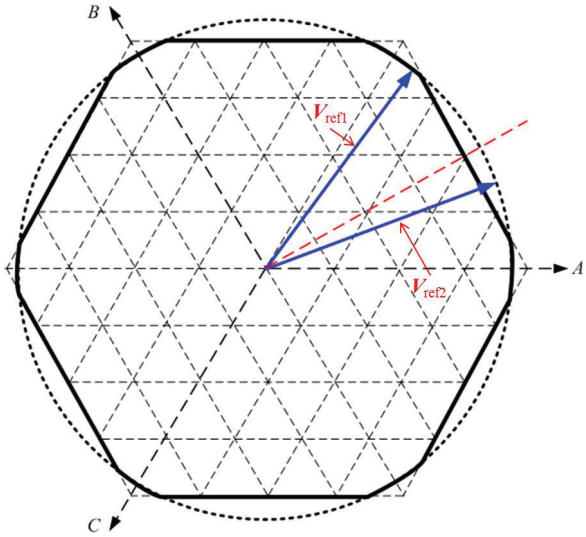



Fig. 10. Modification for reference vectors in over-modulation region

$$r = \mathrm{int}\left(\frac{V_m}{\sqrt{3}V_{dc}/2}\right) + 1 \tag{12}$$

where int($x$) means the integer part of $x$. In this paper, when $r$>$n$-1 ($n$ is the level number of the inverter), the region is called "over-modulation region"; and when 1<$r$<$n$-1, the region is called "low-modulation region".

When the reference vector is in the over-modulation region (e.g., $\boldsymbol{V}_{\mathrm{ref1}}$ or $\boldsymbol{V}_{\mathrm{ref2}}$ in Fig. 10), the proposed SVPWM scheme can easily adjust it to meet different requirements, such as compensation for the loss in volt-second [23] [24]. As an illustration, in this paper the reference vector is modified as

$$\boldsymbol{V}_{ref0} = \min\left\{\frac{\sqrt{3}}{2}V_{dc}(n-1) \Big/ \cos\left(\theta - \frac{1}{6}\pi - \frac{1}{3}\pi \cdot \mathrm{int}\left(\frac{3\theta}{\pi}\right)\right), V_m\right\} \cdot e^{j\theta} \tag{13}$$

where min($x$, $y$) means the smaller value between $x$ and $y$, and $V_m$ and $\theta$ are respectively the magnitude and angle of the original reference vector in (11). Fig. 10 shows an example of the modification in (13); the trajectory of the original reference vectors is the dashed-line circle, and the trajectory after the modification is in bolded lines.

Due to the classification in (12), when the reference vector is in low-modulation regions (1<$r$<$n$-1), the reference vector can be treated as in a ($r$+1)-level space vector diagram instead of in a $n$-level space vector diagram, which is very useful when the level number of the inverter is high while the modulation index of the reference vector is low because less vertex vectors need to be determined. For example, after the classification in (12), the calculation of switching states for the reference vector in Fig. 6 with a relatively low modulation index is shown in Fig. 11. Three vertex vectors need to be produced without classifying the modulation region as in Fig. 6, while only one vertex vector is produced after the classification as in Fig. 11. Generally, for a $k$-level space vector diagram, there are ($k$-2) vertex vectors need to be generated in order to locate the reference vector. Because of the classification, when the reference vector is in the low-modulation regions, fewer vertex vectors, from ($n$-2) to ($r$-1), need to be determined, which makes the SVPWM scheme more efficient, especially when $r$ is much smaller than $n$.

Fig. 12 shows the output phase voltages of a nine-level inverter according to different redundant switching sequences when the reference vectors are located in a low-modulation region (modulation index $m$=0.8) [25]. According to the analysis in section II, when the modulation index is 0.8, there are three switching states at the first vertex of the modulation triangle based on Table I, and consequently there are two redundant switching sequences for each switching sequence mode based on Table II. The letters "U" and "L" in Fig. 12 have the same meanings as in Table II and represent the order number (starts from 1 and numbered from top to bottom) of the

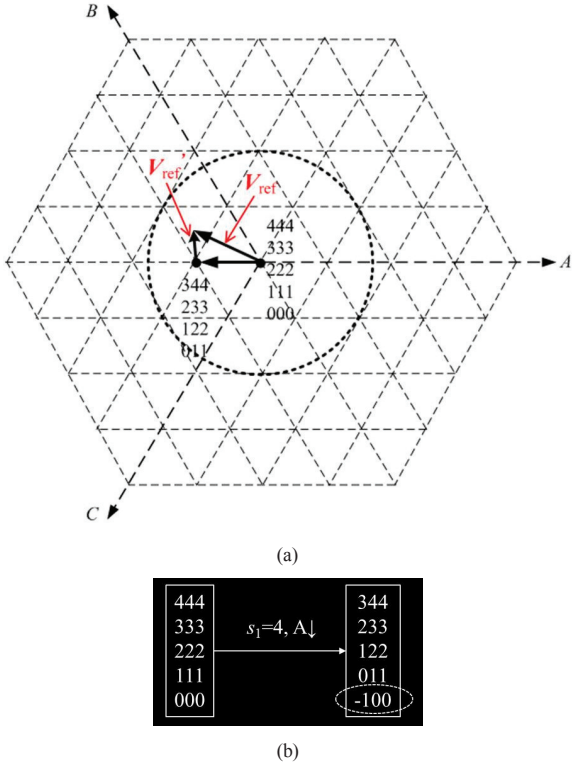



Fig. 11. A reference vector with low modulation index after classifying the modulation region: (a) Locating the reference vector; (b) Calculating the switching states.

first switching state of each switching sequence among all the redundant switching states at the first vertex of the modulation triangle. For example, the switching states 344, 233, 122, and 011 at vertex $P_4$ in Fig. 2 are numbered as 1 to 4, respectively. As before, the switching frequency is 5 kHz (fundamental frequency is 50 Hz), the duty cycles of the two zero vectors are set as $T_{01}$=$T_{02}$=$T_0$/2 in (10), and the switching sequence mode is changed (alternately from one mode to the other) after every switching cycle. Though the different redundant switching sequences in Fig. 12 produce the same line voltage for the nine-level inverter, as shown in Fig. 8, they have different effects on the voltages across the dc-link capacitors of the inverter [19] [21] and thus can be optimally selected to provide

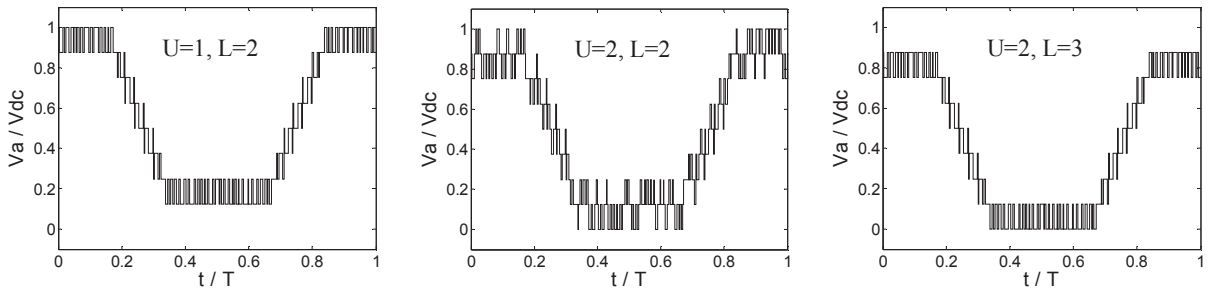



Fig. 12. Normalized PWM voltage waveforms of phase A of a nine-level inverter for different redundant switching sequences ($m$=0.8)

TABLE V

RULE OF THE DETERMINATION OF SWITCHING SEQUENCES (FOR SYMMETRIC SWITCHING SEQUENCE)

| | *reg* | | | | | |
|---|---|---|---|---|---|---|
| | 1 | 2 | 3 | 4 | 5 | 6 |
| *mode*=1 | ABC↑CBA↓(L) | CAB↓BAC↑(U) | BCA↑ACB↓(L) | ABC↓CBA↑(U) | CAB↑BAC↓(L) | BCA↓ACB↑(U) |
| *mode*=2 | CBA↓ABC↑(U) | BAC↑CAB↓(L) | ACB↓BCA↑(U) | CBA↑ABC↓(L) | BAC↓CAB↑(U) | ACB↑BCA↓(L) |

the inverter with a better performance.

### B. Switching Sequence for Specific Requirements

The rule of determining the switching sequence represented by the second mapping in Table II can also be extended to produce the switching sequence for other specific requirements, such as the applications where the switching sequence is preferred to be symmetric [26]. For example, if the original switching sequence is $V_0 \rightarrow V_1 \rightarrow V_2 \rightarrow V_0$, then the preferred switching sequence is $V_0 \rightarrow V_1 \rightarrow V_2 \rightarrow V_0 \rightarrow V_2 \rightarrow V_1 \rightarrow V_0$. The extended rule of determining the switching sequence for such applications is summarized in Table V, in which *reg* is the region number of the modulation triangle calculated in (8) and each element of the rule is actually a combination of the corresponding two elements in Table II for the two switching sequence modes. For example, when *reg*=1 and *mode*=1, the rule of determining the switching sequence in Table V is "ABC↑CBA↓(L)". As explained before, the letter "L" means the first switching state of the switching sequence at the first vertex of the modulation triangle is not the top one; the next first three sequential switching states are generated according to the rule "ABC↑" as in Table II when *reg*=1 and *mode*=1, and the next second three sequential switching states are generated according to the rule "CBA↓" as in Table II when *reg*=1 and *mode*=2. Based on the rule in Table V, the switching sequences for the reference vector (*reg*=2) in Fig. 2 according to different switching sequence modes are summarized in Table VI, which can be verified by comparison with the space vector diagram in Fig. 2. Table V is just a simplified example for demonstrating the extensibility of the second mapping, and in real applications it can also be achieved by selecting the appropriate time reference.

TABLE VI

SYMMETRIC SWITCHING SEQUENCES FOR DIFFERENT MODES

| | |
|---|---|
| *mode*=1 | 142 → 141 → 041 → 031 → 041→ 141 → 142 |
| *mode*=2 | 031 → 041 → 141 → 142 → 141→ 041 → 031 |

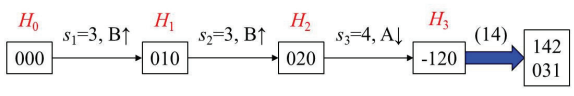



Fig. 13. An alternative way to generate the switching states at the first vertex of the modulation triangle and the vertex vectors

Generally, the switching sequence rule represented by the second mapping in Table II can be conveniently extended to produce the switching sequence for any other specific requirements, as long as the following principle proposed in this paper is applied: 1) when the inverter is switched from one switching state $S_{a1}S_{b1}S_{c1}$ to another $S_{a2}S_{b2}S_{c2}$, the difference between the two vectors represented by $S_{a2}S_{b2}S_{c2}$ and $S_{a1}S_{b1}S_{c1}$ can be substituted into (1) to determine the required modification of $S_{a1}S_{b1}S_{c1}$; 2) for two adjacent switching states in the switching sequence, it is preferred that only the state for one phase is modified.

### C. An Alternative Way to Generate the Switching States

The processing in Fig. 5 of generating the switching states for the vertex vectors can also be implemented in an alternative way as shown in Fig. 13, which can further reduce the computation time. Instead of modifying all the present switching states as in Fig. 5, only one arbitrary switching state (e.g., 000 as in Fig. 13) at the center of $H_0$ is modified for each vertex vector, and finally a candidate switching state $S_aS_bS_c$ (e.g., -120 as in Fig. 13) is produced for the first vertex of the modulation triangle. Based on the obtained switching state $S_aS_bS_c$, all the available switching states at the first vertex of the modulation triangle can also be generated as

$$\{N + S_a, N + S_b, N + S_c\}, \text{ where } N \text{ is an integer} \quad (14a)$$

$$-\min(S_a, S_b, S_c) \le N \le n - 1 - \max(S_a, S_b, S_c) \quad (14b)$$

where $n$ is the level number of the inverter, and $\min(S_a, S_b, S_c)$ and $\max(S_a, S_b, S_c)$ respectively means the minimum and maximum value among $S_a$, $S_b$, and $S_c$. Accordingly, Fig. 13 shows the results of the valid switching states (i.e., 142 and 031) at the first vertex of the modulation triangle, which agree with Fig. 5.

### D. Comparison with Earlier Methods

Table VII (where $n$ is the level number of the inverter) summarizes a detailed comparison between the proposed SVPWM scheme and typical earlier methods, which reveals that the proposed SVPWM scheme is more advanced than the prior methods, in terms of time complexity, space complexity, flexibility of optimizing switching patterns, and suitability. The method in [27] is the conventional method, which detects the modulation triangle, solves three simultaneous equations for

TABLE VII

COMPARISON BETWEEN THE PROPOSED SVPWM SCHEME AND EARLIER METHODS

| SVPWM methods | Time complexity① | Space complexity② | All the switching states are generated? | Method for switching sequences? | Duty cycles adjustable? | Suitable for over-modulation? |
|---|---|---|---|---|---|---|
| In [27] | $O(n^2)$ | $O(n^3)$ | No method is provided | Lookup table | No | No |
| In [11] | $O(n)$ | $3n$ | Yes | No | Yes | No |
| In [12] | $O(n)$ | $O(n^3)$ | Yes | Lookup table | Yes | Yes |
| In [13] | $O(n)$ | $O(n^3)$ | No method is provided | Lookup table | No | No |
| In [14] | $O(n)$ | $O(n^3)$ | No method is provided | Lookup table | Yes | No |
| In [15] | $O(n)$ | $7n$ | No | Yes | Yes | No |
| In this paper | $O(n)$ | $n$ | Yes | Yes | Yes | Yes |

①Since the prior methods need to determine the switching states for all three the vertexes of the modulation triangle in order to generate the switching sequences, the time complexity only considers the complexity for generating the switching states. In other words, if the computation of switching sequences is taken into account, the SVPWM scheme proposed in this paper will relatively have an even better time complexity (i.e., less computation time) because for this scheme, only the switching states for one vertex of the modulation triangle need to be obtained before determining all the redundant switching sequences.

②When evaluating the space complexity, the earlier methods are assumed to be able to generate all the switching sequences based on the stored switching states.

①, ②For both the time complexity and space complexity, only the amount depending on $n$ is counted. Because the schemes in [13] and [14] do not provide the method for generating switching states, the first mapping proposed in this paper is applied to those two schemes when evaluating the time complexity.

the duty cycles, and obtains the switching states and switching sequences from lookup tables, whereas the algorithms described in [11]-[15] are simplified methods.

Compared to the conventional method [27], of which the time complexity is $O(n^2)$ due to detecting the modulation triangle, the proposed SVPWM scheme and the prior simplified methods [11]-[15] achieve a better time complexity, $O(n)$, and are compared in more detail as follows. For the SVPWM scheme in this paper, two equations (15) and (16) in the Appendix and a modification based on the first mapping (Table I) are calculated for each vertex vector to modify the switching states. Since only the switching states at the first vertex of the modulation triangle need to be generated, considering the worst case, i.e., $r \geq n-1$ in (12), the time complexity (number of computations) of the proposed SVPWM scheme is $3n$. The time complexity of the methods described in [13] and [14] is $4n$ because of the rotation of the $d$-$q$ plane in [13] and the two-phase to three-phase transformation in [14] at each step. For the methods introduced in [11] and [15], the switching states are calculated similarly from (14) and the switching states for all the three vertices of the modulation triangle need to be calculated, so the time complexity of those methods is $3n$.

Similarly, since the switching sequences in this paper are generated based on the second mapping (Table II), only the switching states at the first vertex of the modulation triangle need to be stored in memory and thus the space complexity (number of stored switching states) of the proposed SVPWM scheme is $n$. The space complexity of the method in [11] is $3n$, considering the memory for the switching states at the three vertices of the modulation triangle. In order to generate all the switching states based on the method introduced in [15], the switching states of the inner two-level hexagon (including the origin) need to be stored in memory and accordingly the space complexity is $7n$. The space complexity for the other methods is $O(n^3)$ because all the switching states have to be stored.

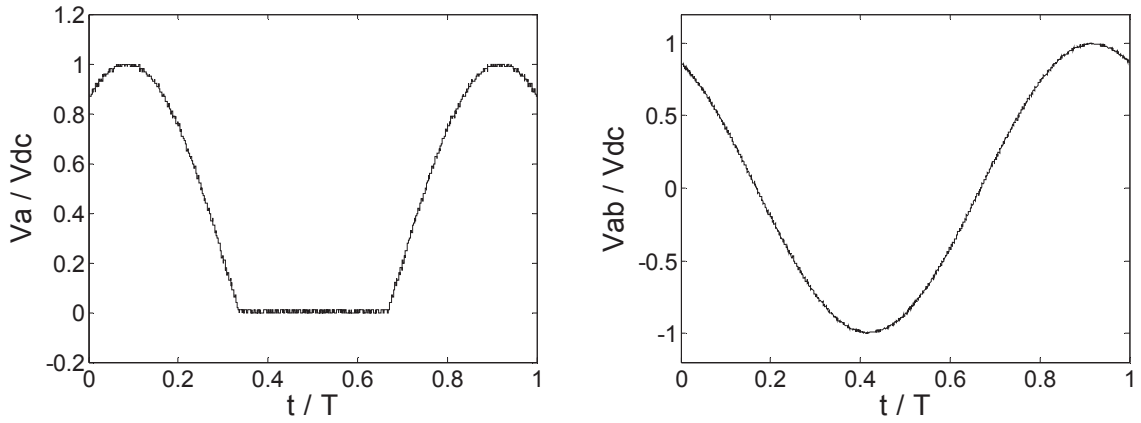
Table VII shows that the time complexity of the method described in [11] is close to the proposed SVPWM scheme, but the method in [11] needs more memory and does not provide a systematic approach for determining the switching sequences or work for the over-modulation regions. The comparison between the other methods and the proposed SVPWM scheme can be summarized similarly according to Table VII.

## IV. EXPERIMENTAL RESULTS

Experiments for a 101-level inverter based on a low-cost Altera Cyclone III field-programmable gate array (FPGA) and the corresponding simulations are presented in this section to validate the proposed SVPWM scheme. The FPGA implements the SVPWM scheme in real time for any received command reference voltage, and digital-to-analog converters (DAC) outputs are applied to observe the output voltages of the inverter.

For the experiments and simulations, the switching frequency $f_s$ is 12.8 kHz (fundamental frequency is 50 Hz), the modulation index of the reference vector is 0.995, the duty cycles of the two zero vectors are set as $T_{01}=T_{02}=T_0/2$ in (10), and the switching sequence mode is changed (alternately from one mode to the other) after every switching cycle. The internal clock of the FPGA is 3.2768 MHz (i.e., 256 * $f_s$).

Fig. 14 shows the simulated output phase voltage (phase A) and line voltage (phase A to phase B) for the 101-level inverter, and Fig. 15 demonstrates the corresponding experimental results. The test results are consistent with the simulation waveforms and indicate the easy implementation of the




(a) (b)

Fig. 14. Simulation results of a 101-level inverter: (a) Output voltage of phase A; (b) Line voltage (phase A to phase B).

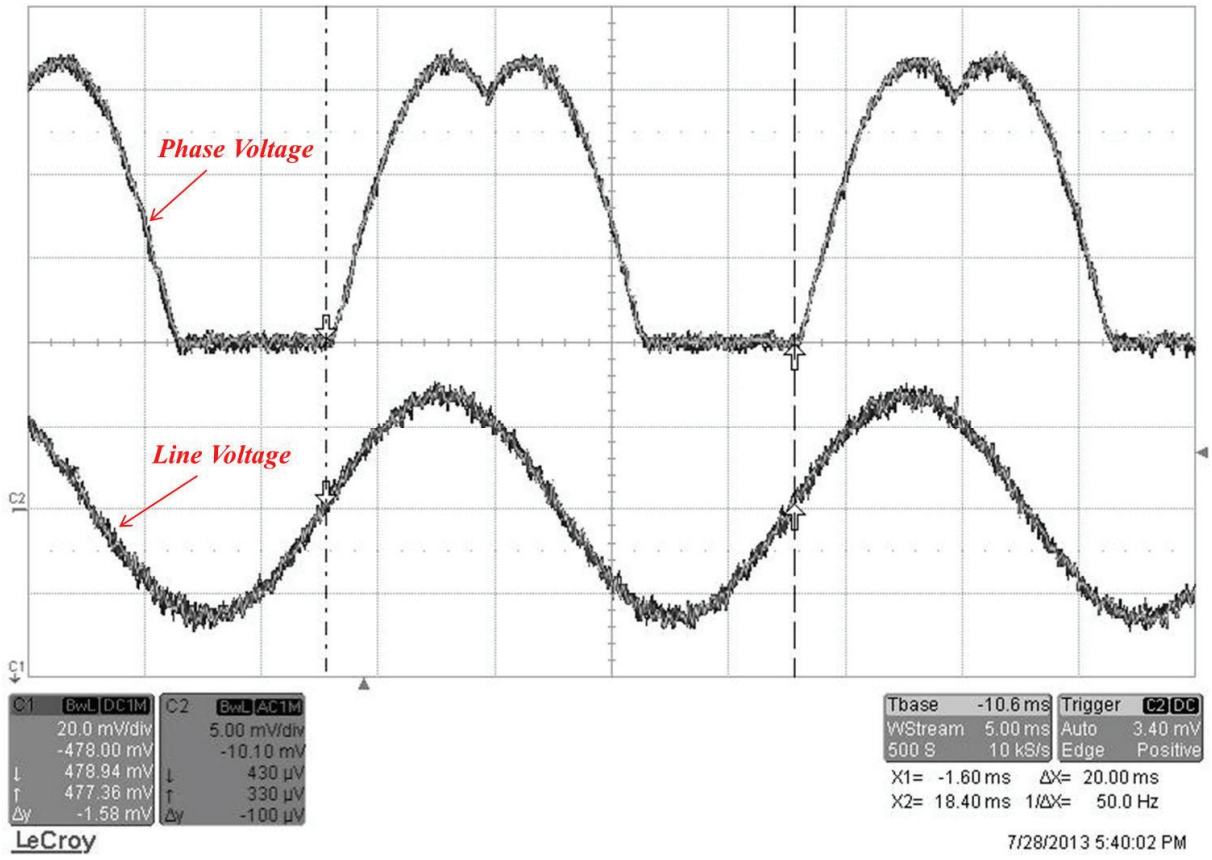



Fig. 15. Experimental results of the output phase voltage (phase A) and line voltage (phase A to phase B) for a 101-level inverter base on a FPGA

proposed SVPWM scheme, even when the level number of the inverter is high.

## V. Conclusion

This paper has presented a new space vector pulse width modulation (SVPWM) scheme for multilevel inverters, which generates all the available switching states and switching sequences based on two simple general mappings, and calculates the duty cycles of the nearest three vectors simply as for a two-level SVPWM, thus independent of the level number of the inverter. Experimental results for a 101-level inverter on a FPGA and simulation results verify the SVPWM scheme.

The proposed SVPWM scheme has the following significant advantages compared with prior SVPWM schemes: 1) switching states, duty cycles, and switching sequences are all obtained by simple calculation, so no lookup table and less memory is needed and the scheme is computationally fast; 2) Compared to earlier methods, the SVPWM scheme proposed in this paper provides two more degrees of freedom, i.e., the adjustable switching sequences and duty cycles; 3) all the available switching states and switching sequences can be obtained, which provides the most flexibility of optimizing switching sequence; 4) the scheme works well for any reference vector with any modulation index, and can be conveniently extended to meet specific requirements; and 5) the proposed scheme is suitable for any level inverter. A more detailed comparison between the proposed SVPWM scheme and prior methods is given. The advantages of this SVPWM scheme make it a useful tool for further study of multilevel inverters.

## Appendix

For any new reference vector $\boldsymbol{V}_{\mathrm{ref(k)}}$ calculated in (5), the corresponding function $s$ obtained from (6) can also be generated by (15), shown at the bottom of the page, where $V_{\mathrm{rx(k)}}$ and $V_{\mathrm{ry(k)}}$ respectively represent the real and imaginary part of $\boldsymbol{V}_{\mathrm{ref(k)}}$. Accordingly, (5) can be re-expressed as

$$\boldsymbol{V}_{ref(k+1)} = \boldsymbol{V}_{ref(k)} - V_{dc} \cdot e^{j(s_{k+1}-1)\pi/3} \tag{16}$$

The region number, *reg*, of the modulation triangle containing the remainder vector $\boldsymbol{V}_{\mathrm{ref}}'$ in (8) can also be calculated as

$$reg = \begin{cases} 1, \ \textbf{if } \left(V_{rx} > 0 \textbf{ and } 0 \le V_{ry} < \sqrt{3}V_{rx}\right); \\ 6, \ \textbf{else if } \left(V_{rx} > 0 \textbf{ and } -\sqrt{3}V_{rx} \le V_{ry} < 0\right); \\ 3, \ \textbf{else if } \left(V_{rx} < 0 \textbf{ and } 0 < V_{ry} \le -\sqrt{3}V_{rx}\right); \\ 4, \ \textbf{else if } \left(V_{rx} < 0 \textbf{ and } \sqrt{3}V_{rx} < V_{ry} \le 0\right); \\ 2, \ \textbf{else if } \left(V_{ry} > 0\right); \\ 5, \ \textbf{else}. \end{cases} \tag{17}$$

where $V_{\mathrm{rx}}$ and $V_{\mathrm{ry}}$ represent the real and imaginary part of $\boldsymbol{V}_{\mathrm{ref}}'/V_{\mathrm{dc}}$, respectively.

## Acknowledgment

Y. Deng would like to thank the Mitsubishi Electric Research Laboratories (MERL), Cambridge, MA for their support, as the primary work was done at MERL when he was a research intern.

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$$s_{k+1} = \begin{cases} 1, \ \textbf{if } \left(V_{rx(k)} > 0 \textbf{ and } -\frac{\sqrt{3}}{3}V_{rx(k)} \le V_{ry(k)} < \frac{\sqrt{3}}{3}V_{rx(k)}\right); \\ 2, \ \textbf{else if } \left(V_{rx(k)} > 0 \textbf{ and } V_{ry(k)} \ge \frac{\sqrt{3}}{3}V_{rx(k)}\right); \\ 3, \ \textbf{else if } \left(\left(V_{rx(k)} < 0 \textbf{ and } V_{ry(k)} > -\frac{\sqrt{3}}{3}V_{rx(k)}\right) \textbf{ or } \left(V_{rx(k)} = 0 \textbf{ and } V_{ry(k)} > 0\right)\right); \\ 4, \ \textbf{else if } \left(V_{rx(k)} < 0 \textbf{ and } \frac{\sqrt{3}}{3}V_{rx(k)} < V_{ry(k)} \le -\frac{\sqrt{3}}{3}V_{rx(k)}\right); \\ 5, \ \textbf{else if } \left(V_{rx(k)} < 0 \textbf{ and } V_{ry(k)} \le \frac{\sqrt{3}}{3}V_{rx(k)}\right); \\ 6, \ \textbf{else}. \end{cases} \tag{15}$$

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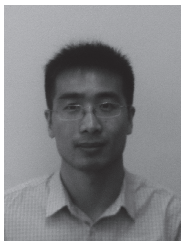

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