A 5-Level Efficient IFPWM Power Coding Approach Encoding LTE for Class-S Digital-RF Transmitter with Distortion Correction

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A 5-Level Efficient IFPWM Power Coding Approach Encoding LTE for Class-S Digital-RF Transmitter with Distortion Correction

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Abstract — In this work, for the first time we propose a multi-level intermediate frequency pulse width modulation (ML-IFPWM) power coding approach to generate a high speed pulse train as input of GHz class-S switch-mode PA in the digital-RF transmitter. The key feature of a high power coding efficiency of 68.5% from a 5-level digitally implemented discrete-time (DT)-PWM quantizer encoding 20-MHz LTE signal (PAR of 10.25-dB) is verified by simulation. Unlike the traditional RFPWM, this new power coding process taking place at IF frequency of 100 MHz, offers a higher over-sampling ratio thus resulting in an improved output spectrum purity. In addition, a look-up-table based linearization unit is introduced in the digital-RF transmitter architecture to specifically correct the distortion caused by the nonlinear transformation of power encoder. To the author's knowledge, this is the most efficient power coding approach in a digital implementation reported so far encoding 20-MHz LTE at 2 GHz with low EVM of 4.1%.

Index Terms — Digital-RF transmitter, multi-level encoder, power coding efficiency, pulse width modulator (PWM), microwave power amplifiers, switch-mode PA.

I. INTRODUCTION

Advanced switch-mode power amplifiers (SMPAs), e.g. class-S, have become one of the key power amplifier architectures under intensive research in recent years [1]. The benefits of high theoretical power efficiency and operational flexibility manifest themselves as very promising enablers for the next generation digital-RF transmitter (TX) in software-defined radio (SDR).

Fig. 1 shows the architecture of a digital-RF TX utilizing class-S as the final stage to efficiently amplify a high speed pulse-train generated via power encoder, like delta sigma modulator (DSM) [1], pulse width modulator (PWM) [2]-[3], or pulse position modulator (PPM) [4]. Normally a high-Q (>500) bandpass filter (BPF) is needed to reconstruct the signal back to analog RF. Notably, with the recent advancement of GaN RF transistor technology, this architecture is gaining more attention, in particular for small base station cellular applications.

However, the very low "**power coding efficiency**" (*defined by authors specifically as a ratio of the desired in-band power to the entire band power of the digitized signal, to clearly distinguish from the coding efficiency mentioned normally in information theory*) of the conventional power encoders handling communication signals with high peak-to-average-ratio (PAR>8dB) is one of the most critical

factors affecting the power efficiency of the TX, as the SMPA needs to wastefully amply quite large portion of the useless out-of-band noise. So far, the most widely adopted power encoder (e.g. DSM) achieves in practice only limited power coding efficiency (<30%). This is attributed to the generation of quantization noise and the noise shaping function for enhancing the in-band SNR.
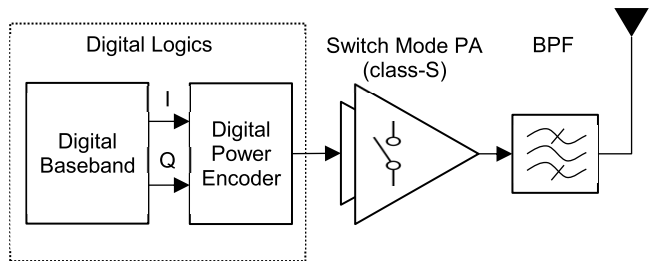

Fig. 1.   Digital-RF transmitter architecture based on SMPA.

Recently, several new power coding schemes based on RFPWM were proposed [2]-[3], reporting improved power coding efficiency. Nevertheless, in order to meet the spectrum linearity requirement, especially for suppressing the in-band noise floor and out-of-band image replicas, the power encoder needs an ultra-fast sampling clock ($50 \times f_{RF}$) to obtain high enough over-sampling ratio of RF at GHz for cellular applications, which is hard to implement using commercial digital processors today.

In this work, we propose a novel encoding scheme of Multi-Level IFPWM (ML-IFPWM) via two-stage digital up-conversion at a dramatically reduced sampling rate whilst also achieving high power coding efficiency. Furthermore, a specially designed linearization unit is introduced. The paper is organized as follows: Section II describes the power coding scheme, Section III evaluates the simulation performance of the ML-IFPWM with LTE signal, and Section IV concludes the work.

II. ML-IFPWM SCHEME

To leverage the advantages of RFPWM and overcome the hardware implementation challenges mentioned above, our proposed power coding approach is consequently realized by decreasing the PWM input frequency to an intermediate frequency (IF, e.g. 100 MHz), and then perform the encoding with Cartesian IF IQ signals by a ML-IFPWM

(see Fig. 2). In this section, the overall ML-IFPWM scheme is introduced first. Then the nonlinearity correction using LUT Pre-Distortion is discussed. And, an exemplary architecture for implementing 5-level IFPWM for SMPA is given in the end.
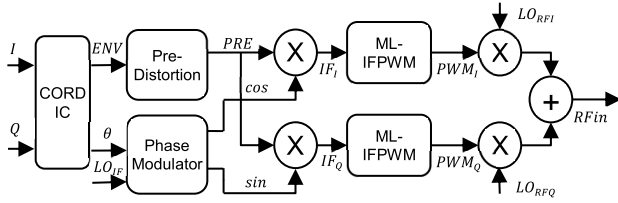

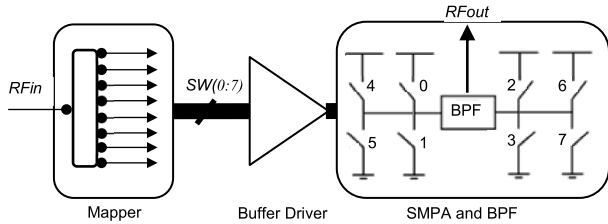Fig. 2.   Proposed ML-IFPWM power coding diagram.

Fig. 3.   SMPA control scheme for 5-level power encoder.

A. ML-IFPWM

As illustrated in Fig. 2, the pre-distorted envelope (see Subsection B), together with the original phase information will recombine at IF (to calculate the IF_I and IF_Q), to feed the IQ IFPWM quantizer. The IFPWM has multiple fixed thresholds, which is simpler than the traditional PWM encoder requiring the generation of triangular or saw tooth reference waveform for comparison. These thresholds are synchronized to the threshold parameters used in the LUT pre-distortion frame by frame.

The key feature of this ML-IFPWM is that the horizontal time domain quantization step is refined by lowering the encoding frequency from RF (GHz) to IF (MHz), which makes the algorithm implementable using commercial available FPGA (e.g. I/O throughput speed of 10 Gbps for IF of 100 MHz). The vertical IQ magnitude quantization is also stretched by adopting multi-level (ML) power coding.

After the ML quantizer, two 4-state digital LOs (i.e., $LO_{RFI}\{..., 1, 0, -1, 0, ...\}$, and $LO_{RFQ}\{..., 0, -1, 0, 1, ...\}$), are used to up-convert the IF IQ signals to RF. At this stage, we set the system sampling rate to be 4 times the RF LO frequency. This clearly reduces the sampling rate requirement compared to the traditional RFPWM. Finally, the generated digital-RF signal for SMPA is:

$$RF_{in} = PWM_I \cdot LO_{RFI} + PWM_Q \cdot LO_{RFQ} \qquad (1)$$

This algorithm can be simply implemented in parallel in the commercial available FPGA (e.g. Xilinx Virtex-7), due to the straightforward pipeline structure (unlike the DSM with feedback loops consuming dramatically increased FPGA resource block and/or speed).

B. LUT Pre-Distortion

It is known that PWM is an inherently nonlinear converter (see (2)). Thus, in order to maintain the signal integrity/linearity, a pre-distortion unit is introduced before the quantization. The LUT block pre-distorts the envelope of baseband IQ signals. It is adaptively configurable to each frame. The pre-distortion approach is described in details as follows.

Firstly, the cumulative distribution function (CDF) of the signal is calculated in each frame. Next, multiple threshold values for each quantization levels should be properly chosen according to the signal CDF. We derive the AM-AM transfer function of the (2N+1)-level quantizer based on the reported 3-level encoding method [4]. For a general (2N+1)-level quantizer, the AM-AM transfer function is,

$$f(a(t)) = \frac{1}{N}\sum_{i=1}^{N} \cos\left[\sin^{-1}\left(\frac{V_{thi}}{a(t)}\right)\right], \ a(t) \geq V_{thN} \quad (2)$$

where $a(t)$ is the envelope, and V_{thi} is the ith threshold value, $V_{thi} < V_{thj}$ when $1 \leq i < j \leq N$. A LUT can be composed to describe the inverse behavior of the nonlinearity of the encoder, which is described in (2). Pre-distortion procedure can be imposed according to the searched LUT value. This LUT searching algorithm has in theory no limitation on the number of quantization level, which is an advantage over the analytical inverse function based pre-distortion scheme [3]. In addition, the SMPA nonlinearity could also be considered and pre-distorted in the baseband.

C. Exemplary ML-IFPWM Architecture

Fig. 3 shows an exemplary architecture of SMPA for an up to 5-level PWM in a digital-RF TX. It consists of mapper, buffer drivers, switching transistors, and a band-pass filter. By properly controlling the ON/OFF states of the switching transistors (SW0-7) via mapper, a 3-/5-level pulse train can be generated based on the extended H-bridge SMPA (SW4-7 having the twice transistor size of SW0-3 for 5-level case).

TABLE I
H-BRIDGE CONTROL FOR 3-LEVEL (GREYED) OR 5-LEVEL

RFin	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
2	0	0	0	0	1	0	0	1
1	1	0	0	1	0	0	0	0
0	0	1	0	1	0	0	0	0
-1	0	1	1	0	0	0	0	0
-2	0	0	0	0	0	1	1	0

III. PERFORMANCE EVALUATION

In order to evaluate the performance of the ML-IFPWM encoder concept, a co-simulation bench has been built using Agilent SystemVue and MATLAB with 5-MHz and 20-MHz high PAR LTE signals at 2 GHz (see Table II).

TABLE II
PERFORMANCE COMPARISON OF POWER CODING SCHEMES

| Scheme	State-of-The-Art					This Work	
	BPDSM [1]		RFPWM [3]		Noise Shaped PPM [4]	IFPWM	
Attribute	2-Level	3-Level	2-Level	3-Level	2-Level	5-Level	
RF Carrier Frequency (GHz)	0.8		2.58		1	1.94	
Digital Clock (GS/sec)	3.2		Discrete Analog		4	7.37	
Modulation Bandwidth (MHz)	1.23		5		20 (Tone-Space)	5	20
Signal Type	5.5dB PAR CDMA		5.6dB PAR WCDMA		Tow-Tone	9.75dB PAR LTE	10.25dB PAR LTE
Power Coding Efficiency	30%	58%	35.5%	67%	28%	75.27%	68.50%
Error Vector Magnitude (EVM)	2.35%	3%	N/A	N/A	N/A	2.45%	4.11%
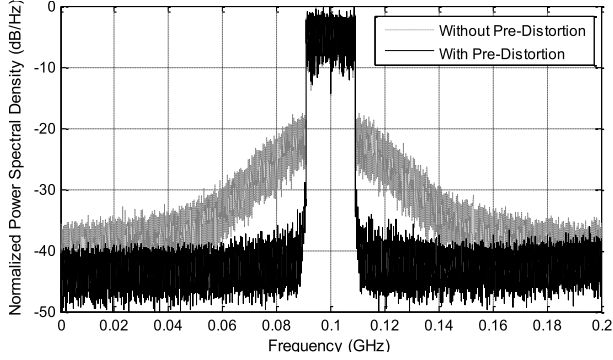
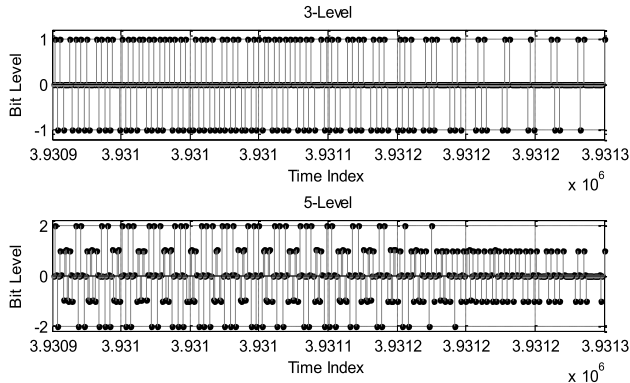Fig. 5. The 5-level IFPWM spectrum w. and w./o. pre-distortion.

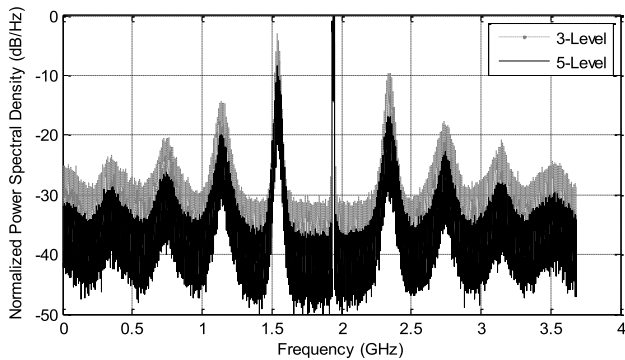Fig. 6. The generated switching pulse-train (3-/5-level).

Fig. 7. The generated switching pulse-train spectrum (3-/5-level).

Approximately 15-dB linearity correction is achieved by the LUT pre-distorter (see Fig. 5). Fig. 6 and Fig. 7 compare the generated high speed pulse train (input signal for SMPA) waveform and spectrum for 3- and 5-level power coding, respectively.

Table II summarizes the performance of the recent publications. Using the 5-level IFPWM encoder, for 20-MHz 10.25dB PAR LTE signal, 68.5% coding efficiency is achieved. To our knowledge, this is the highest power coding efficiency reported. Meanwhile, low EVM (4.11%) is obtained with pre-distortion.

IV. CONCLUSION

A new power coding approach for efficiently encoding a 20-MHz LTE signal with ML-IFPWM is demonstrated for GHz digital-RF TX. Very promising encoding performance in terms of both power coding efficiency and linearity are shown. The investigations of the whole digital-RF TX front-end, focusing on the practical performances of switching transistors are ongoing.

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